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Project Code & Schematics Subject:

PCB P/N:

P. Leader

Check by

Design by

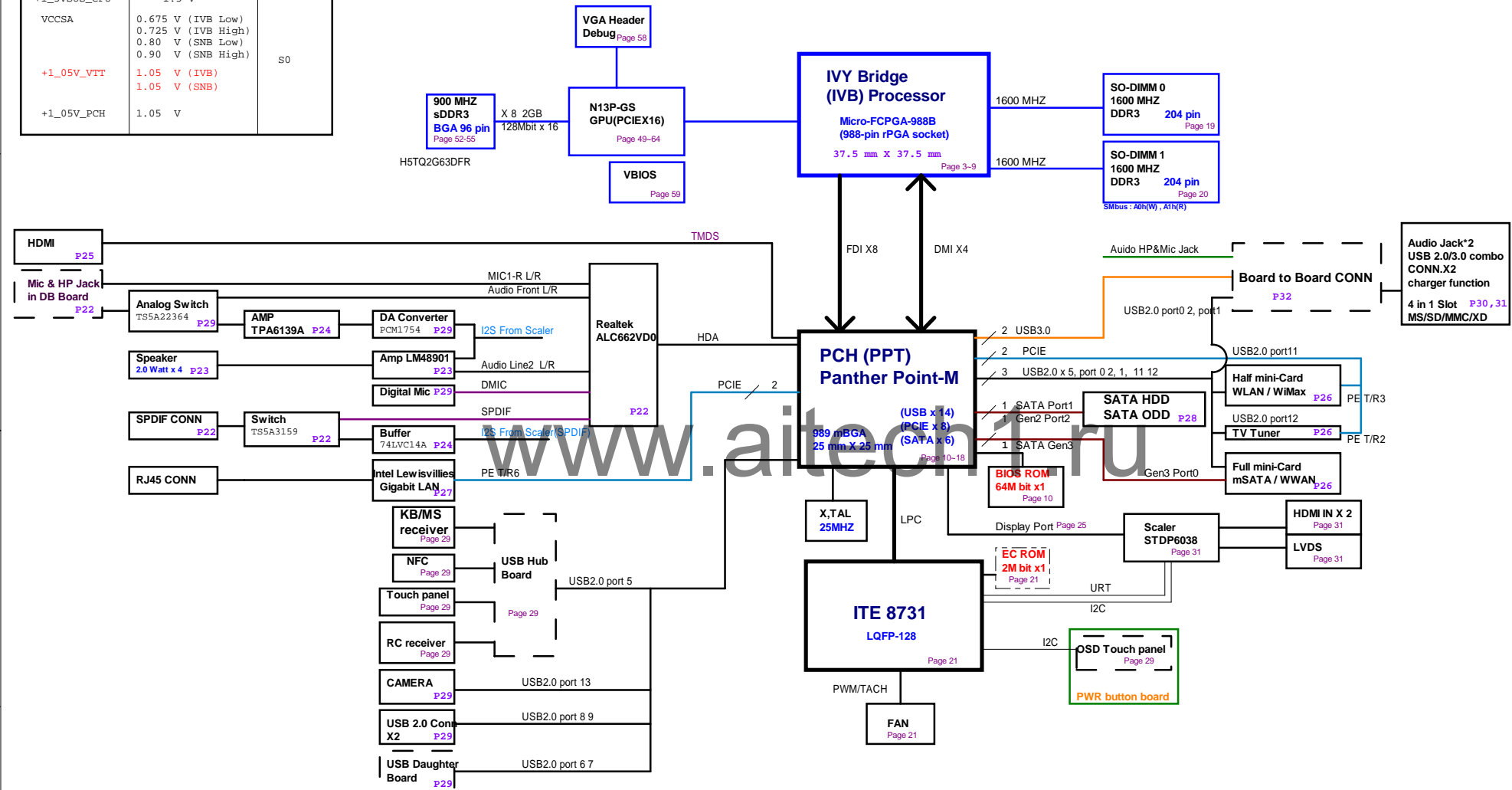
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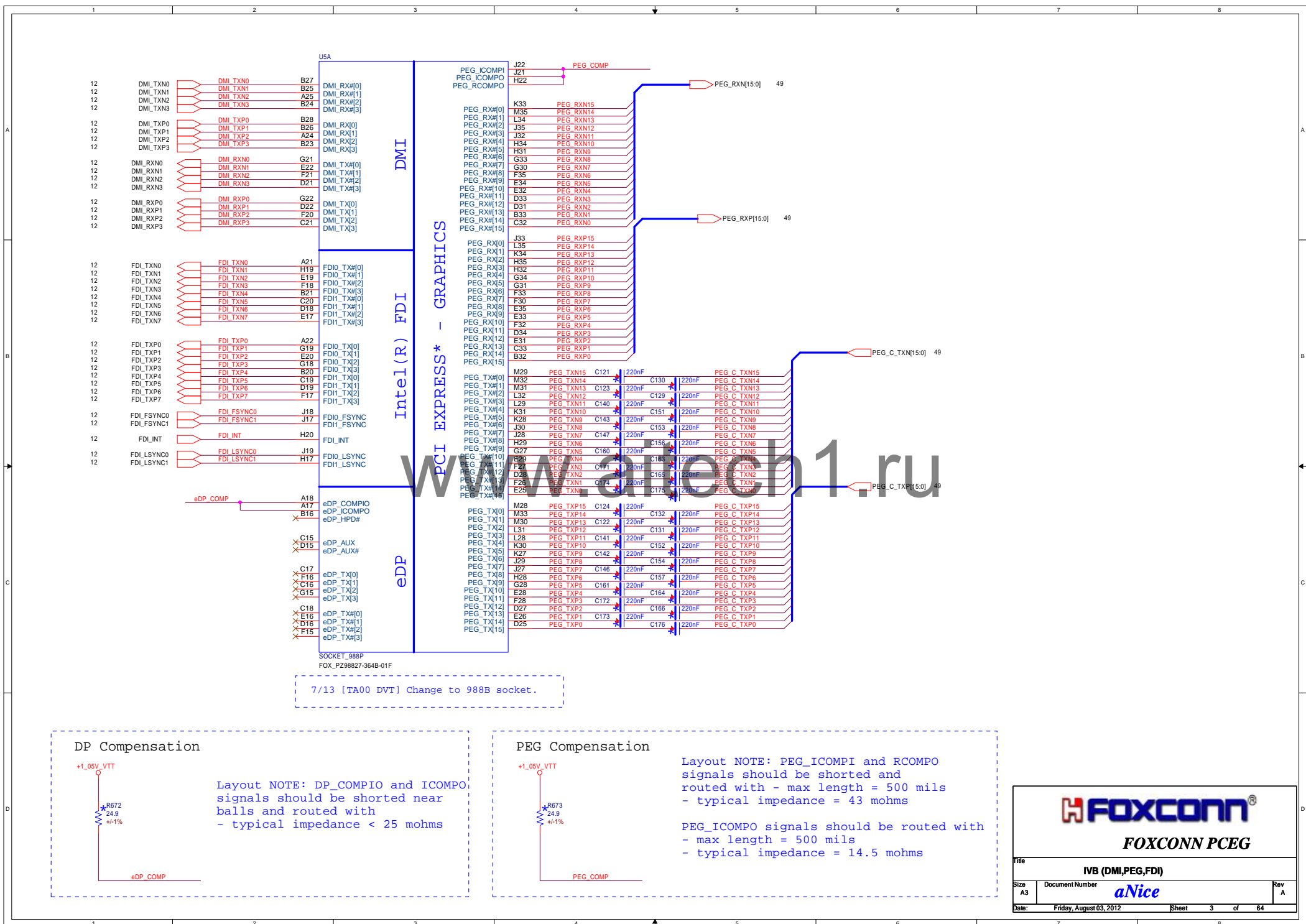
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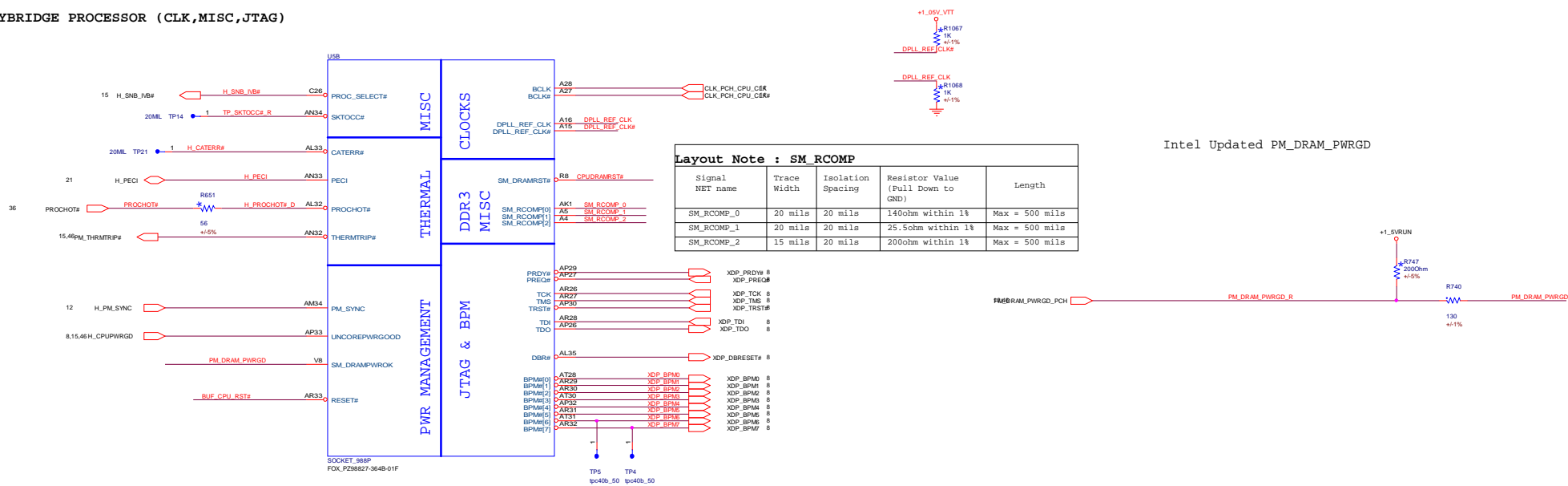
Everest Chief River Platform

POWER PLANE	Voltage	Voltage Rises Active In
+1_5VSUS_CPU	1.5 V	S0
VCCSA	0.675 V (IVB Low) 0.725 V (IVB High) 0.80 V (SNB Low) 0.90 V (SNB High)	
+1_05V_VTT	1.05 V (IVB) 1.05 V (SNB)	
+1_05V_PCH	1.05 V	





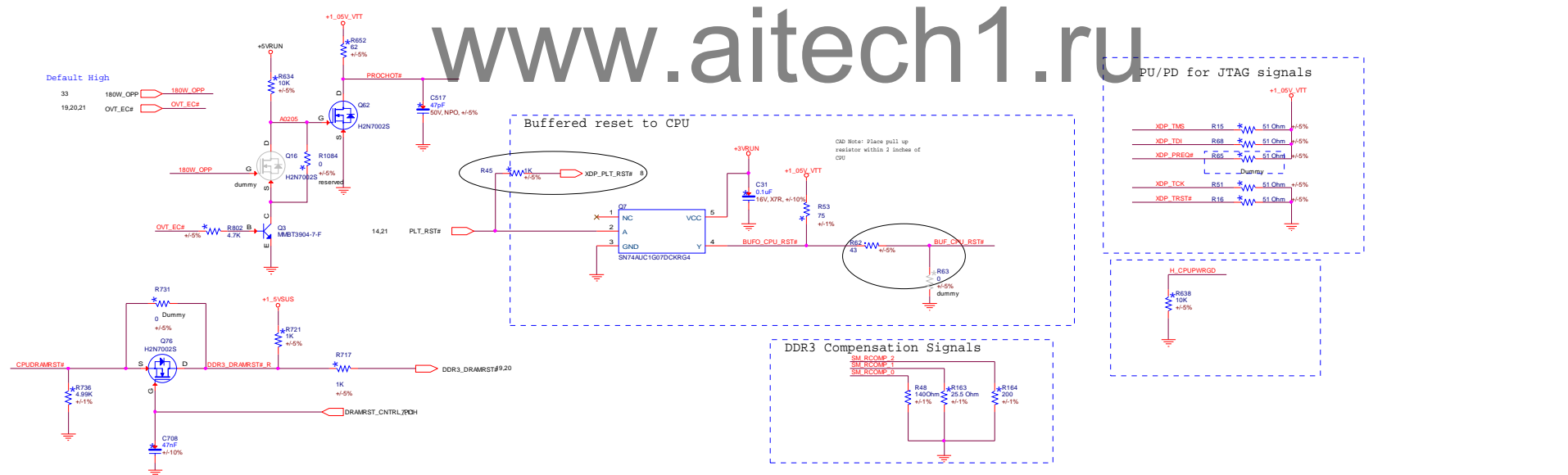
IVYBRIDGE PROCESSOR (CLK,MISC,JTAG)



Layout Note : SM_RCOMP

Signal NET name	Trace Width	Isolation Spacing	Resistor Value (Pull Down to GND)	Length
SM_RCOMP_0	20 mils	20 mils	140ohm within 1λ	Max = 500 mils
SM_RCOMP_1	20 mils	20 mils	25.5ohm within 1λ	Max = 500 mils
SM_RCOMP_2	15 mils	20 mils	200ohm within 1λ	Max = 500 mils

Intel Updated PM_DRAM_PWRGD



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PU/PD for JTAG signals

Buffered reset to CPU

DDR3 Compensation Signals

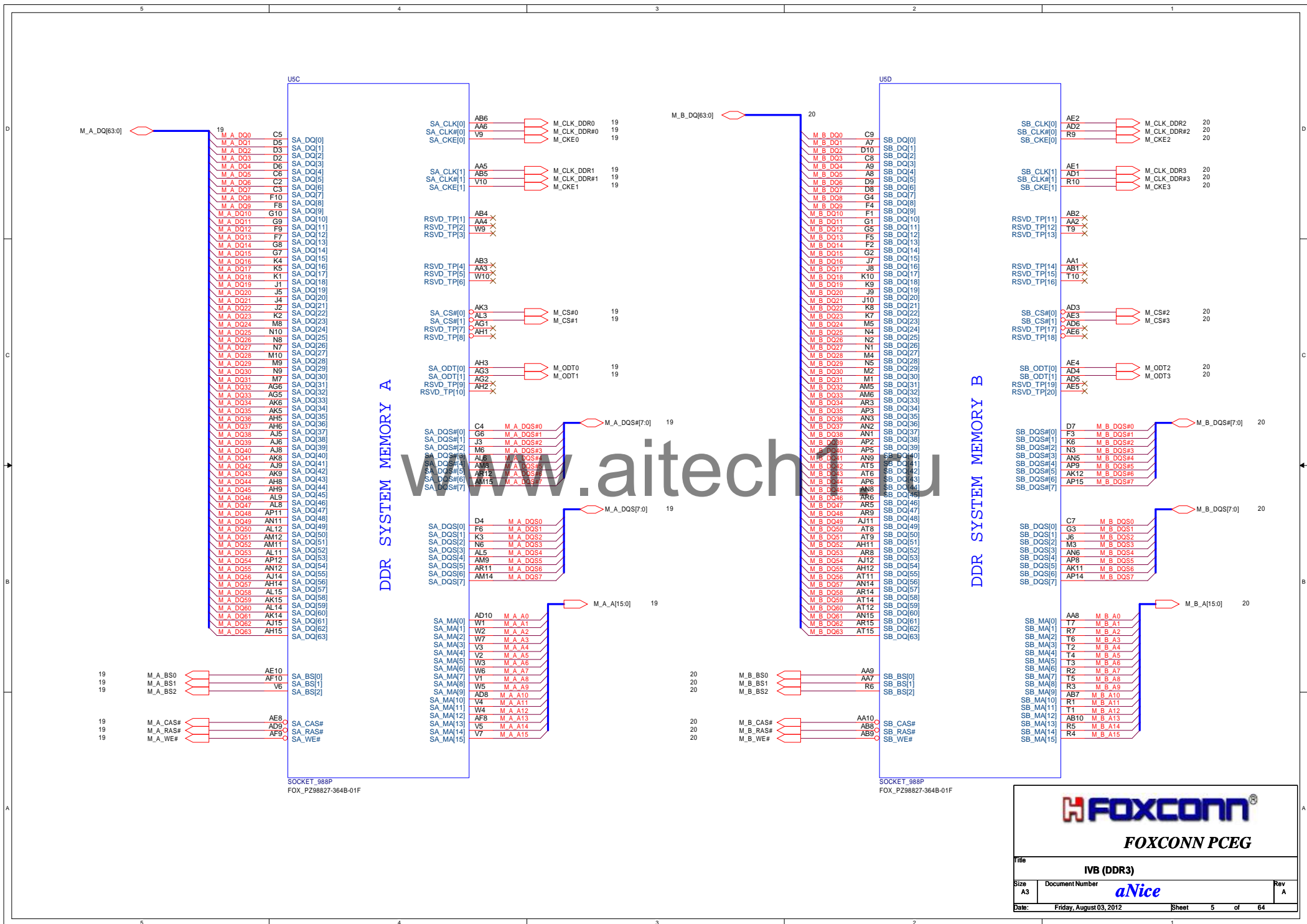


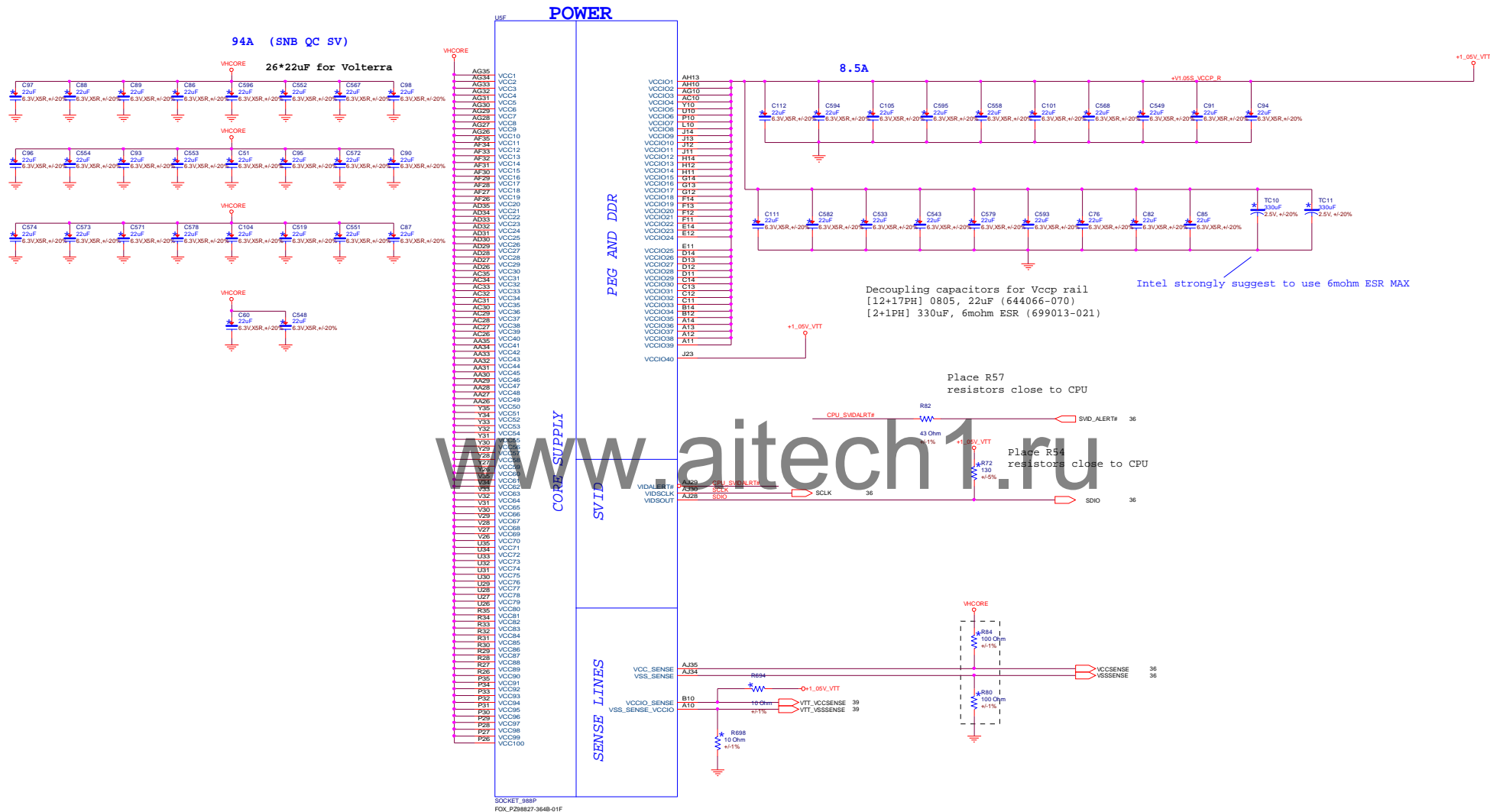
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Title **IVB (CLK,MISC,JTAG)**

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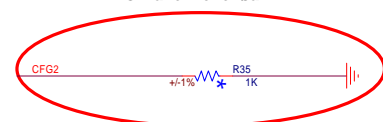
IVB (DDR3)

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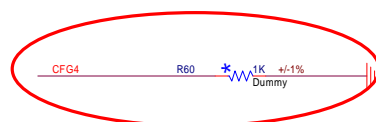
Note: <For PWR IFDIM 代刚>
 TP代號TP1007 TP1008
 い環伏決篤郎 . 硃 癸
 結琇differential結, キ≈i結,
 い i和 嵩跋.

PEG Lane reversal

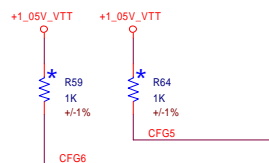


PEG static Lane Reversal - CFG2 is for 16X		
CFG2		
0	LANE Reversed	
1	(Default)Normal Operation	

ENABLE EDP



Display Port Presence Strap		
CFG4		
0	Enabled eDP	
1	(Default)Disabled eDP	



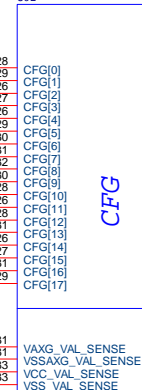
PEG DFER Training		
CFG7		
0	PEG Wait for Bios for Training	
1	(Default)PEG Train immediately following xxResetB Deassertion	

PCIe Port Bifurcation Straps		
CFG[6:5]		
11	(Default)16X	
10	X8 X8	
01	Reserved	
00	X8 X4 X4	

Reserve Circuit

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USE



CFG

RESERVED

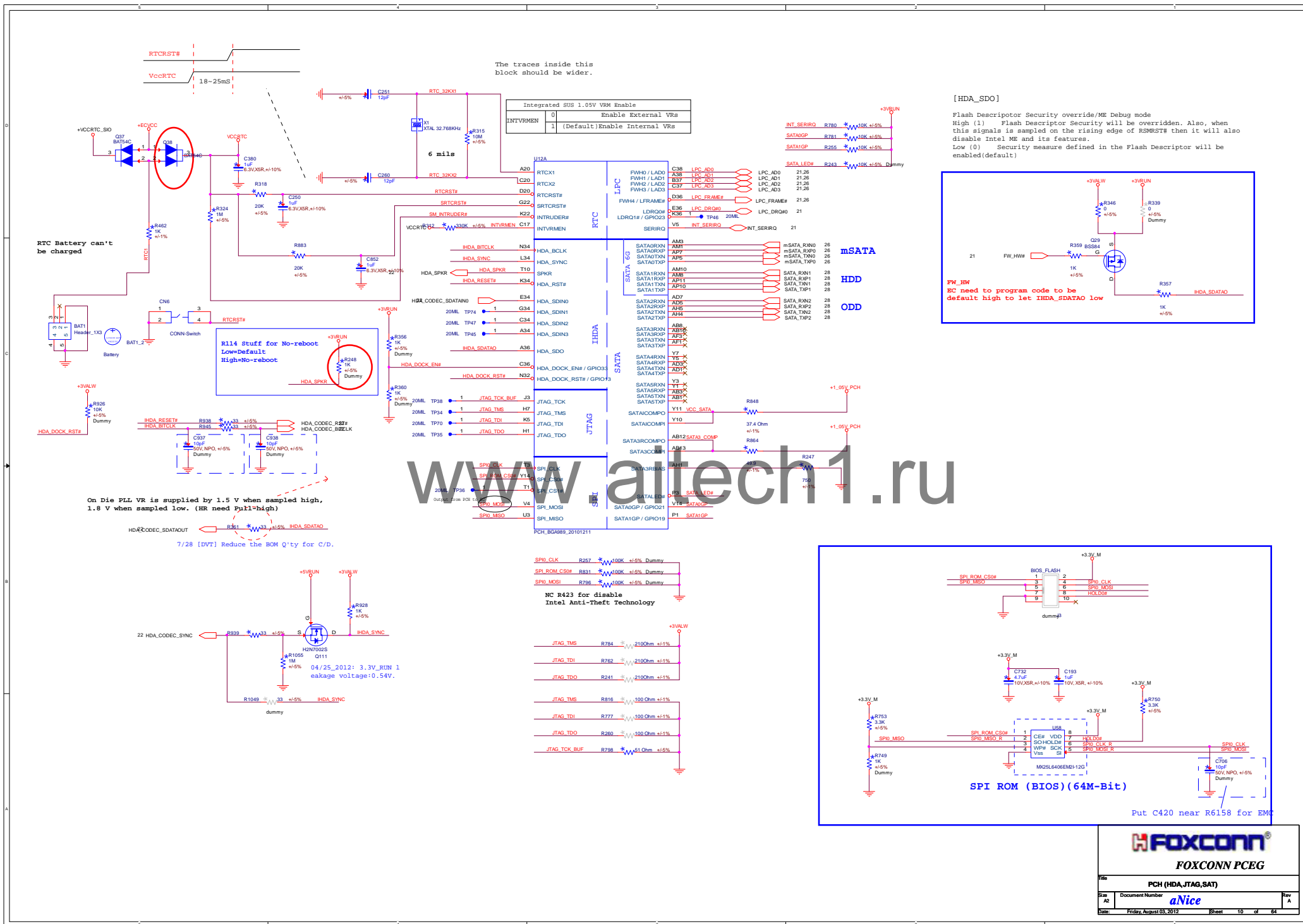


SOCKET_988P
 FOX_P298827-364B-01F



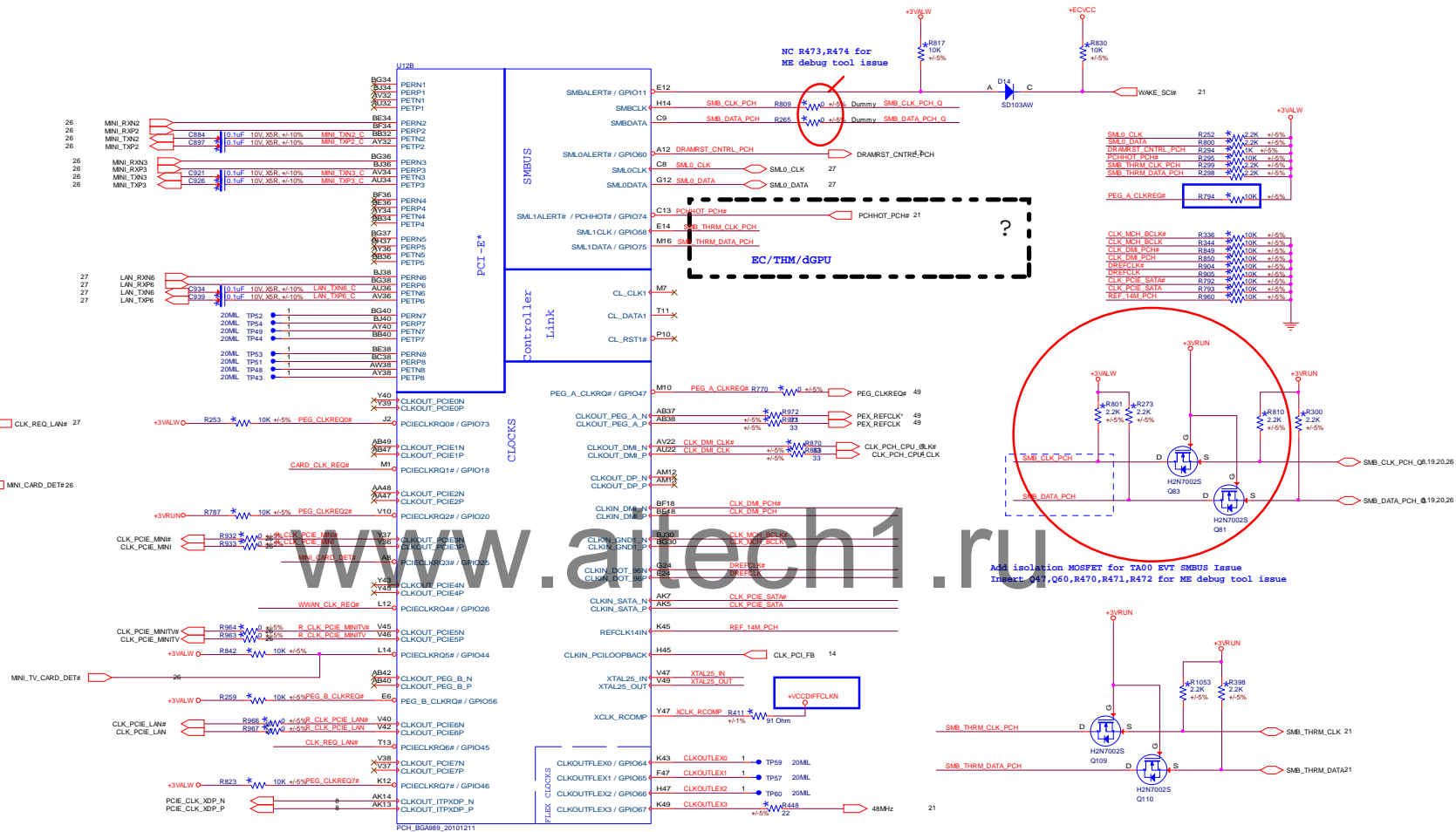
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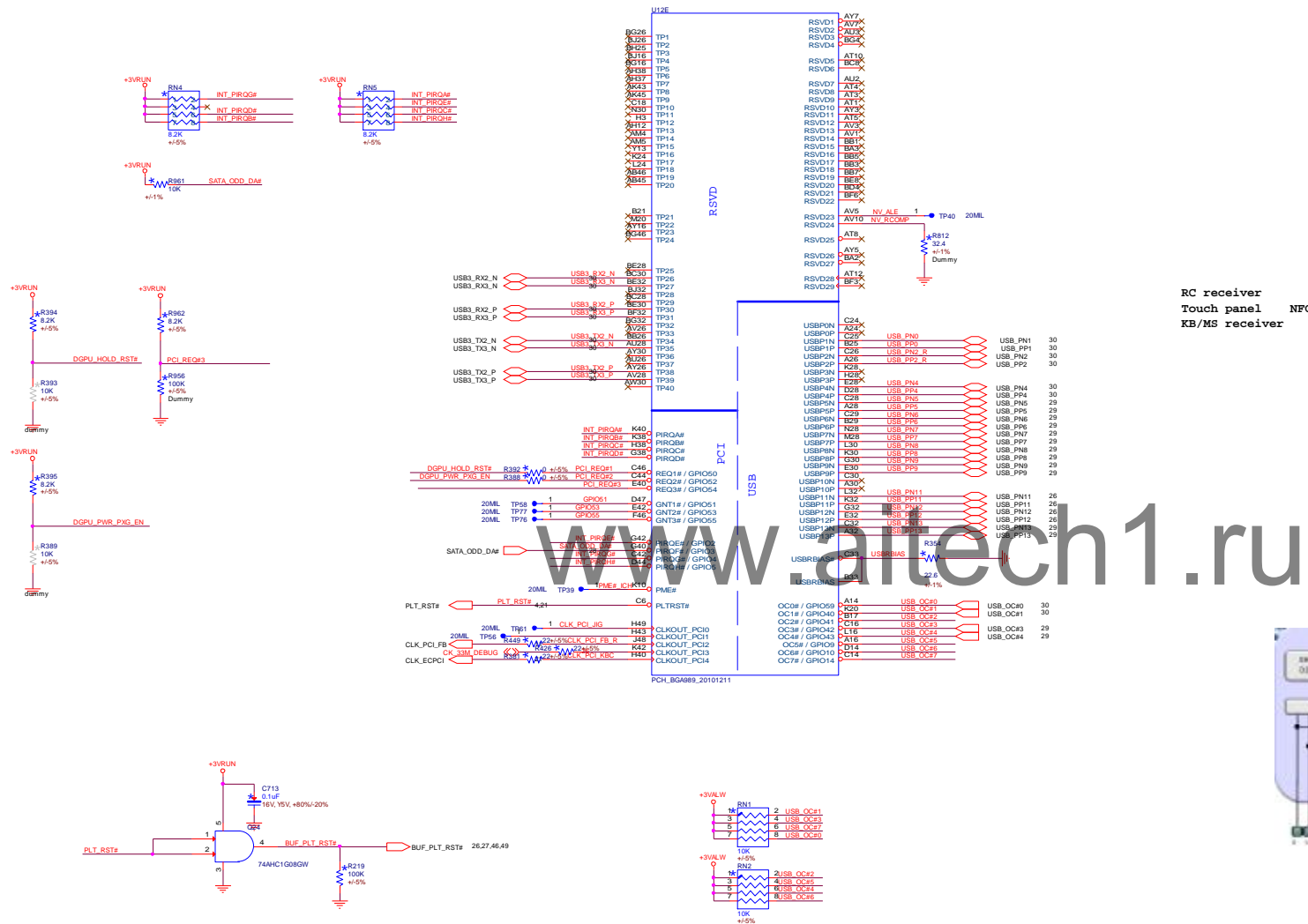
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IVB (RESERVED)			
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PCI-E Port Table

Port	Function
Port1	NC
Port2	ExpressCard/34 (PCI-E)
Port3	WLAN
Port4	NC
Port5	NC
Port6	GbE LAN
Port7	NC
Port8	NC



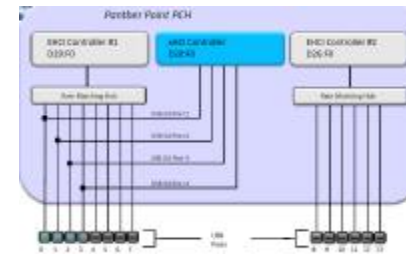


USB PORT	Function
PORT-0	External Port-0 (USB 3.0)
PORT-1	Card Reader
PORT-2	External Port-2 (USB 3.0)
PORT-3	
PORT-4	
PORT-5	USB Hub (USB 2.0)
PORT-6	DB Port-0 (USB 2.0)
PORT-7	DB Port-0 (USB 2.0)
PORT-8	MB Port-0 (USB 2.0)
PORT-9	MB Port-0 (USB 2.0) / debug port
PORT-10	
PORT-11	mini_PCIE-2 (WLAN+BT)
PORT-12	mini_PCIE-3 (TV)
PORT-13	Camera + MIC

RC receiver
Touch panel NFC
KB/MS receiver

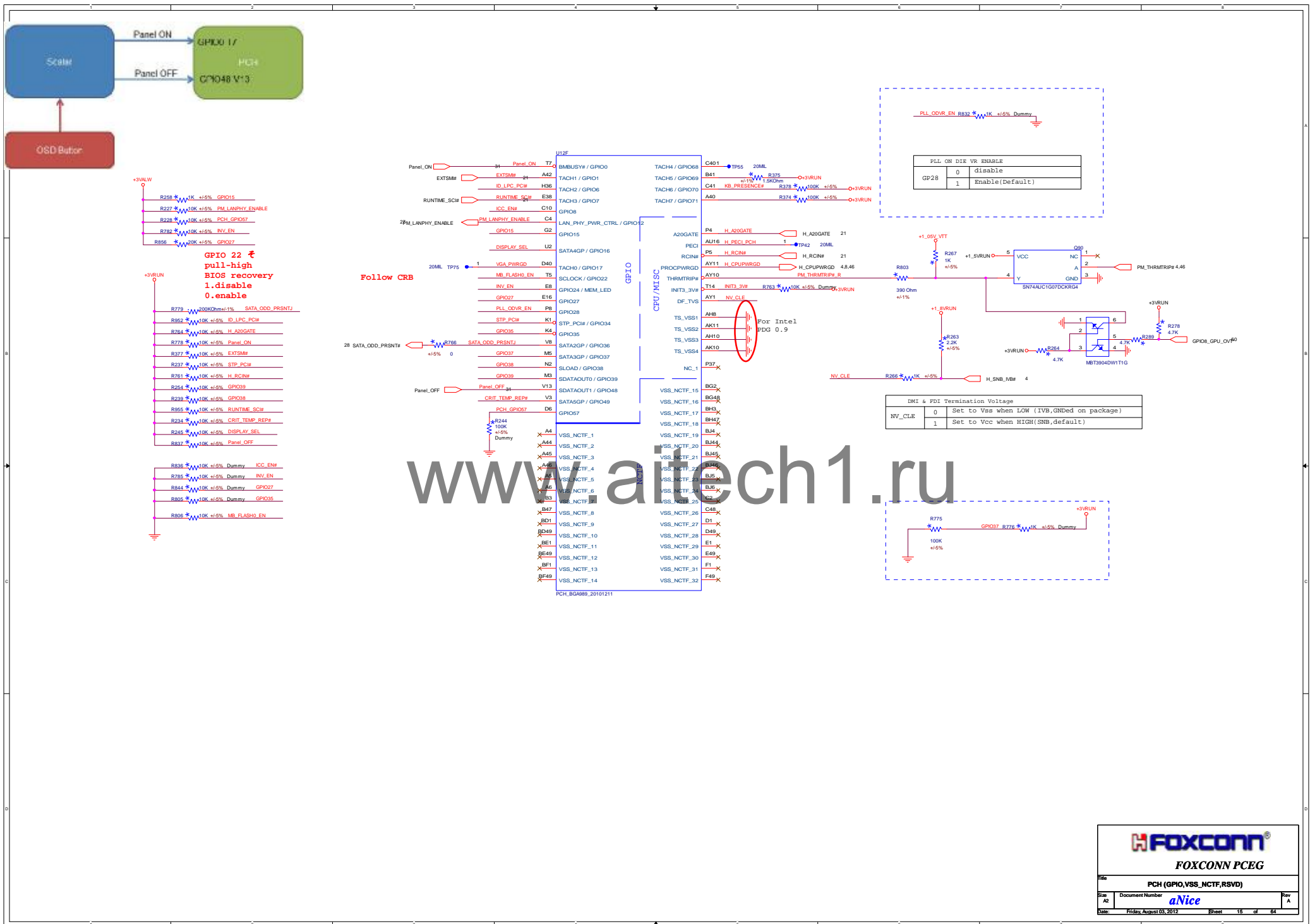
USB 3.0/2.0 Port Pairing

USB 3.0 PORT	USB 2.0 PORT
PORT-1	PORT-0
PORT-2	PORT-1
PORT-3	PORT-2
PORT-4	PORT-3

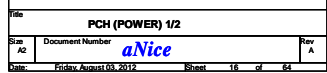
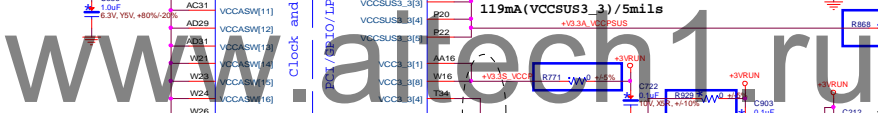


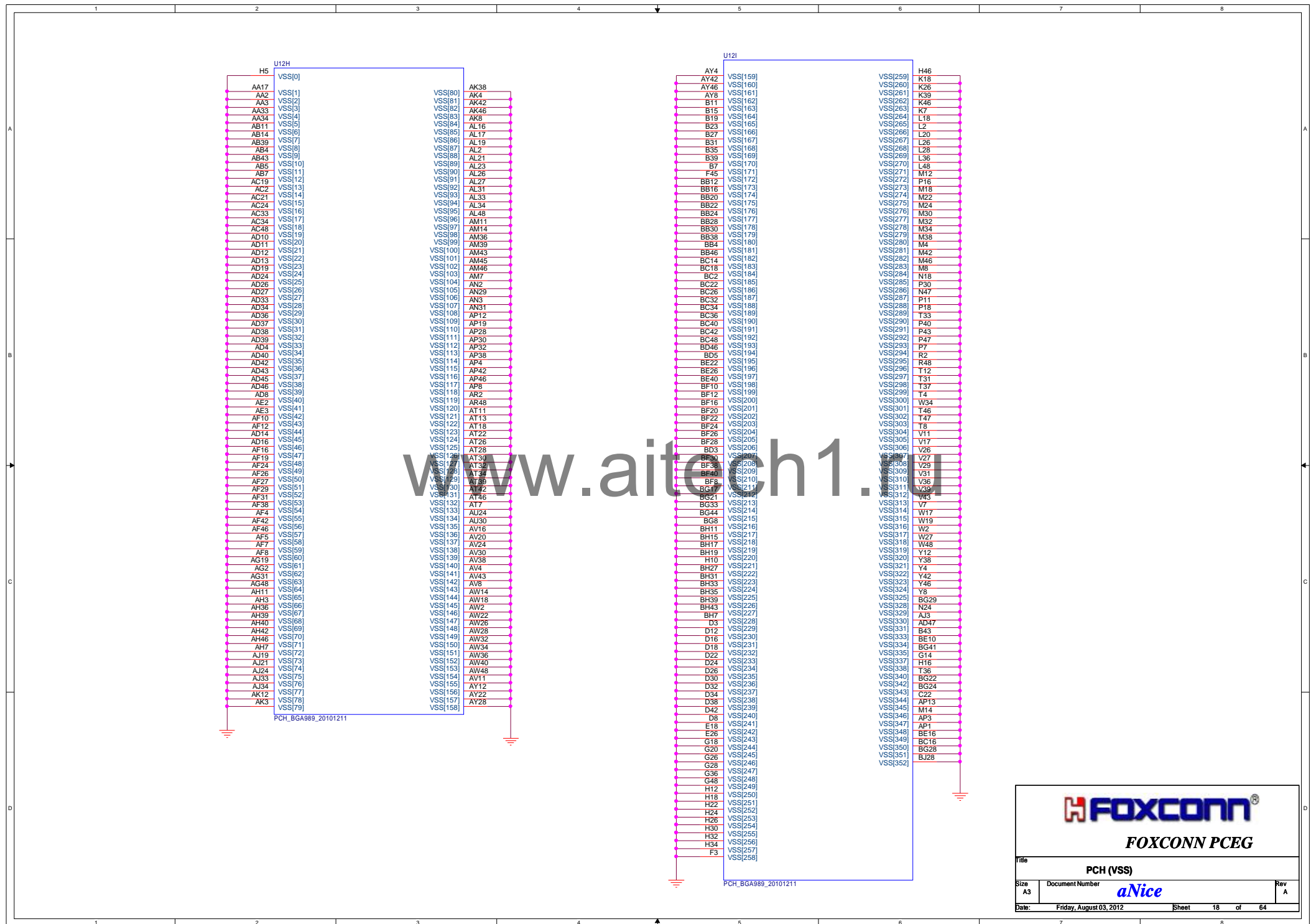
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File: PCH (PCI,USB,NVRAM)		
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CPT do not defined current/20mils



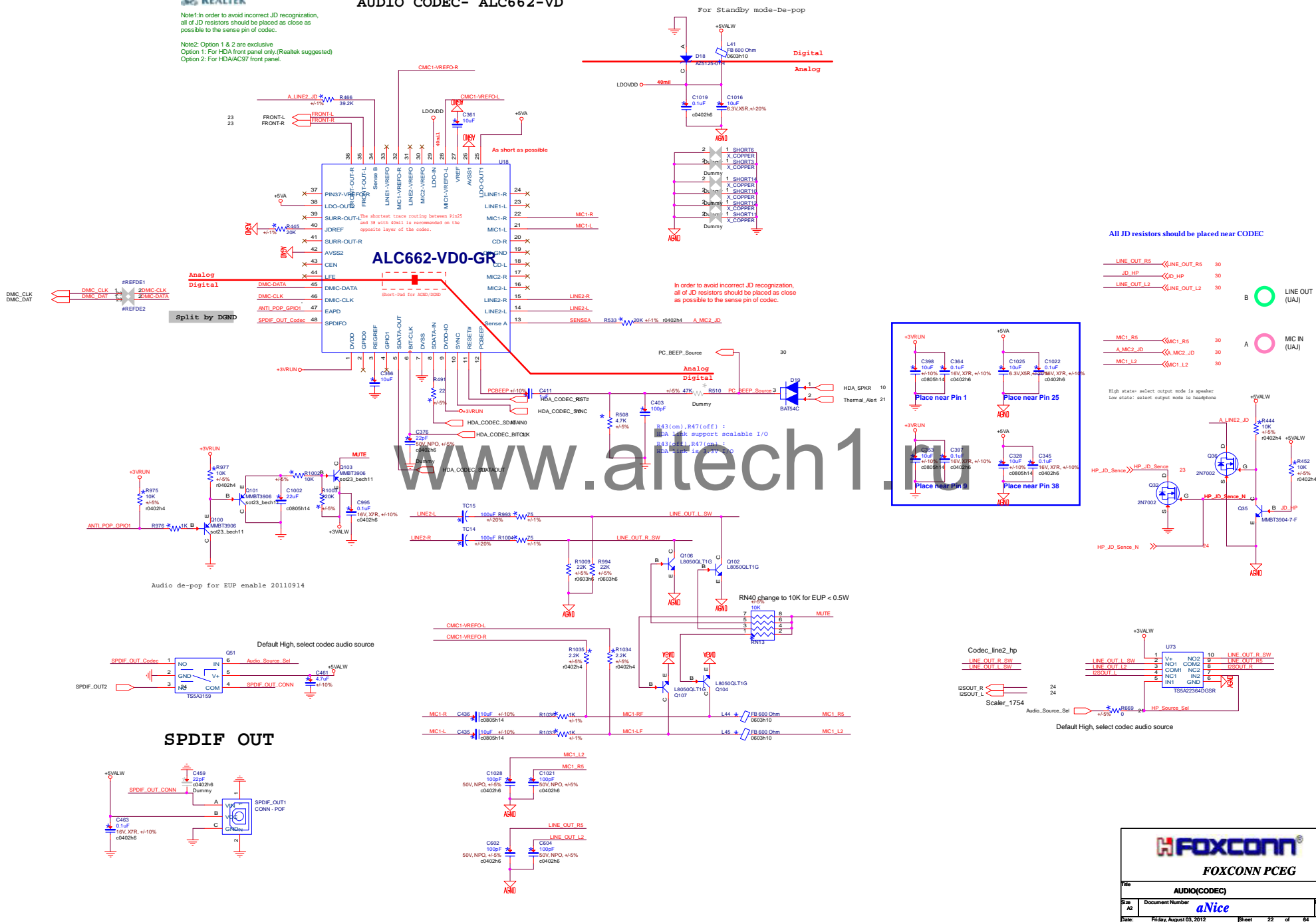


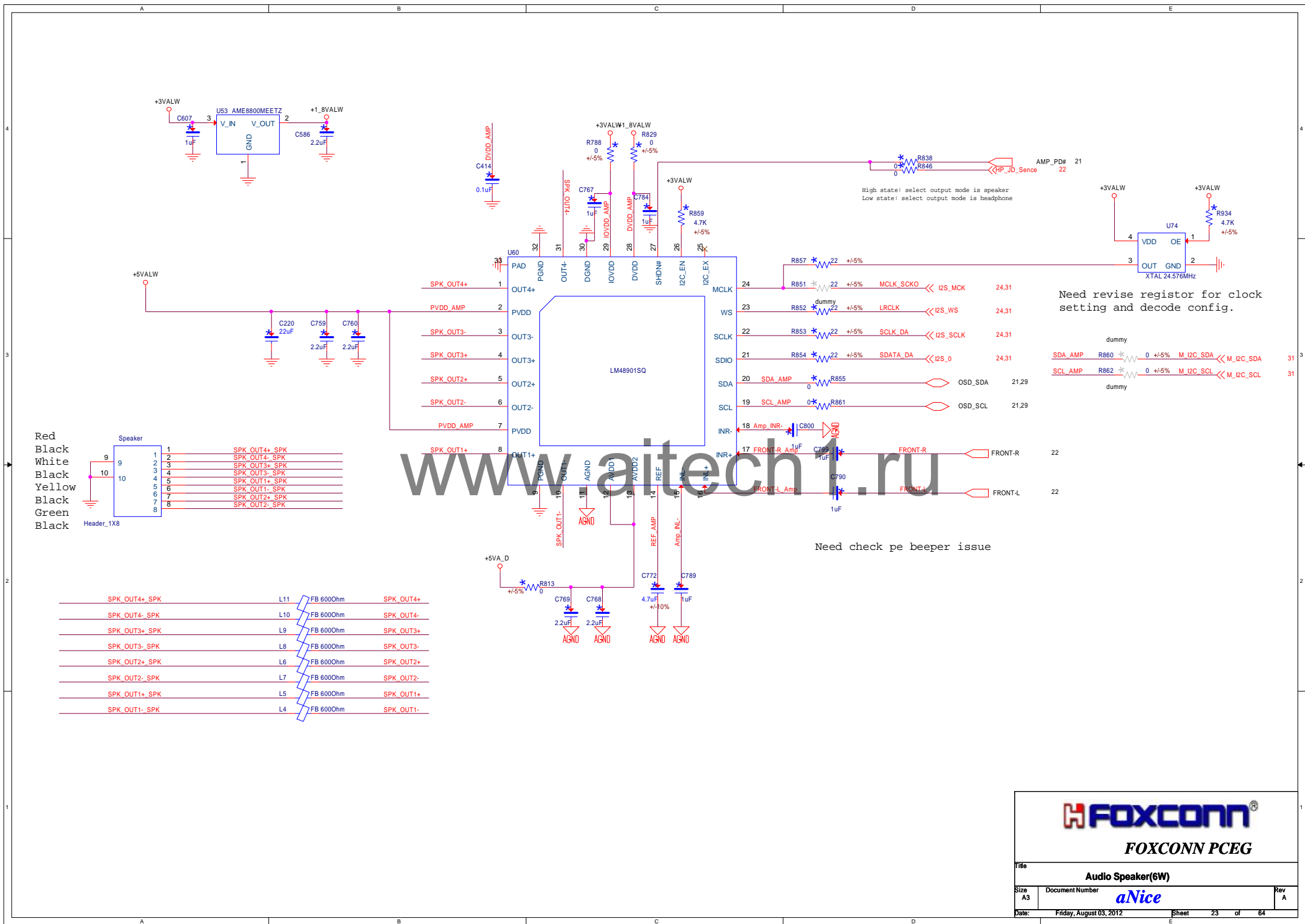
		
Title: PCH (VSS)		
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AUDIO CODEC- ALC662-VD

Note1: In order to avoid incorrect JD recognition, all of JD resistors should be placed as close as possible to the sense pin of codec.

Note2: Option 1 & 2 are exclusive
Option 1: For HDA front panel only.(Realtek suggested)
Option 2: For HDA/AC97 front panel.



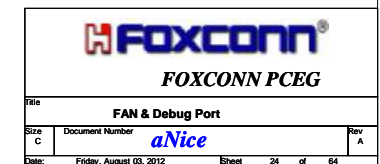


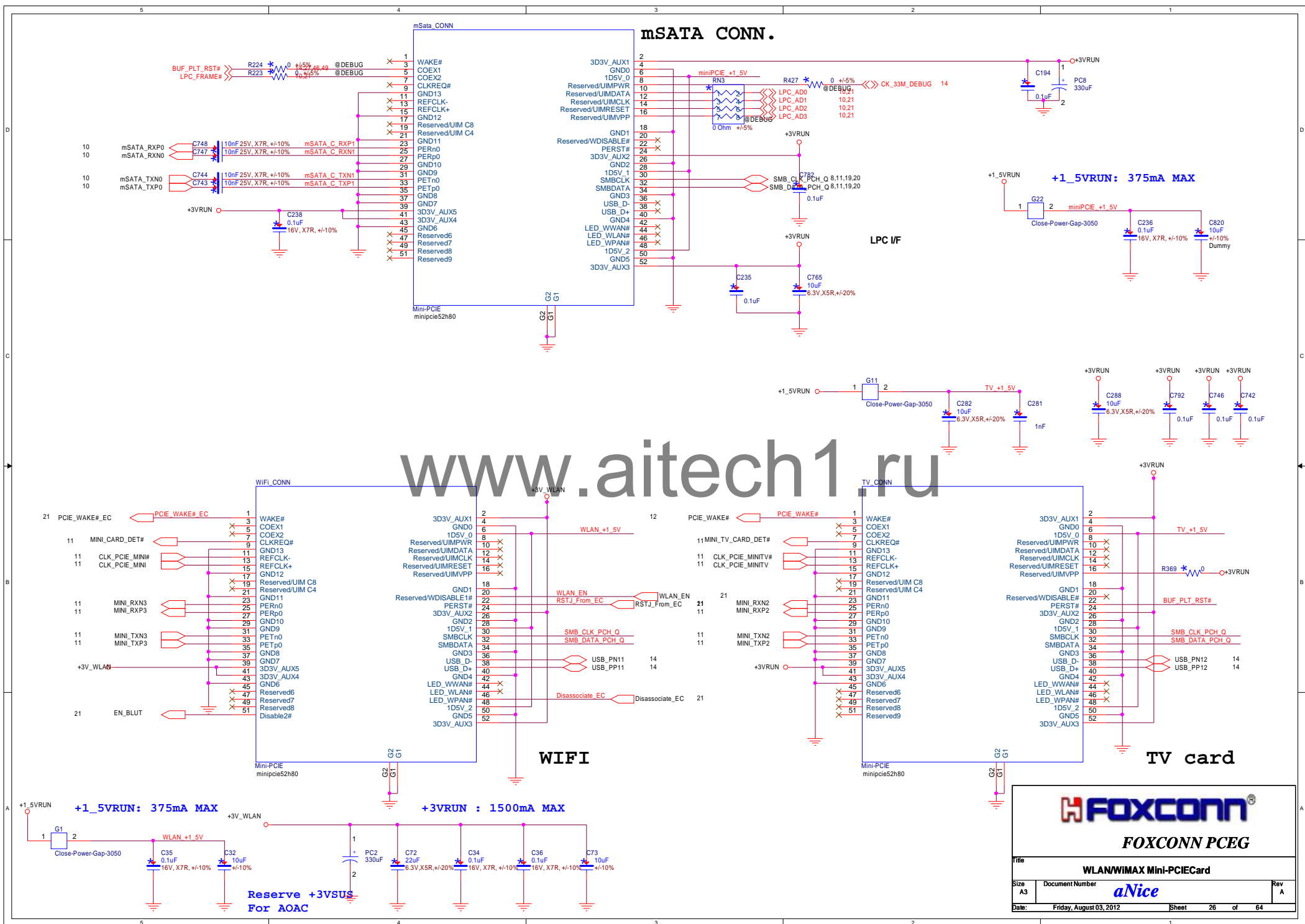
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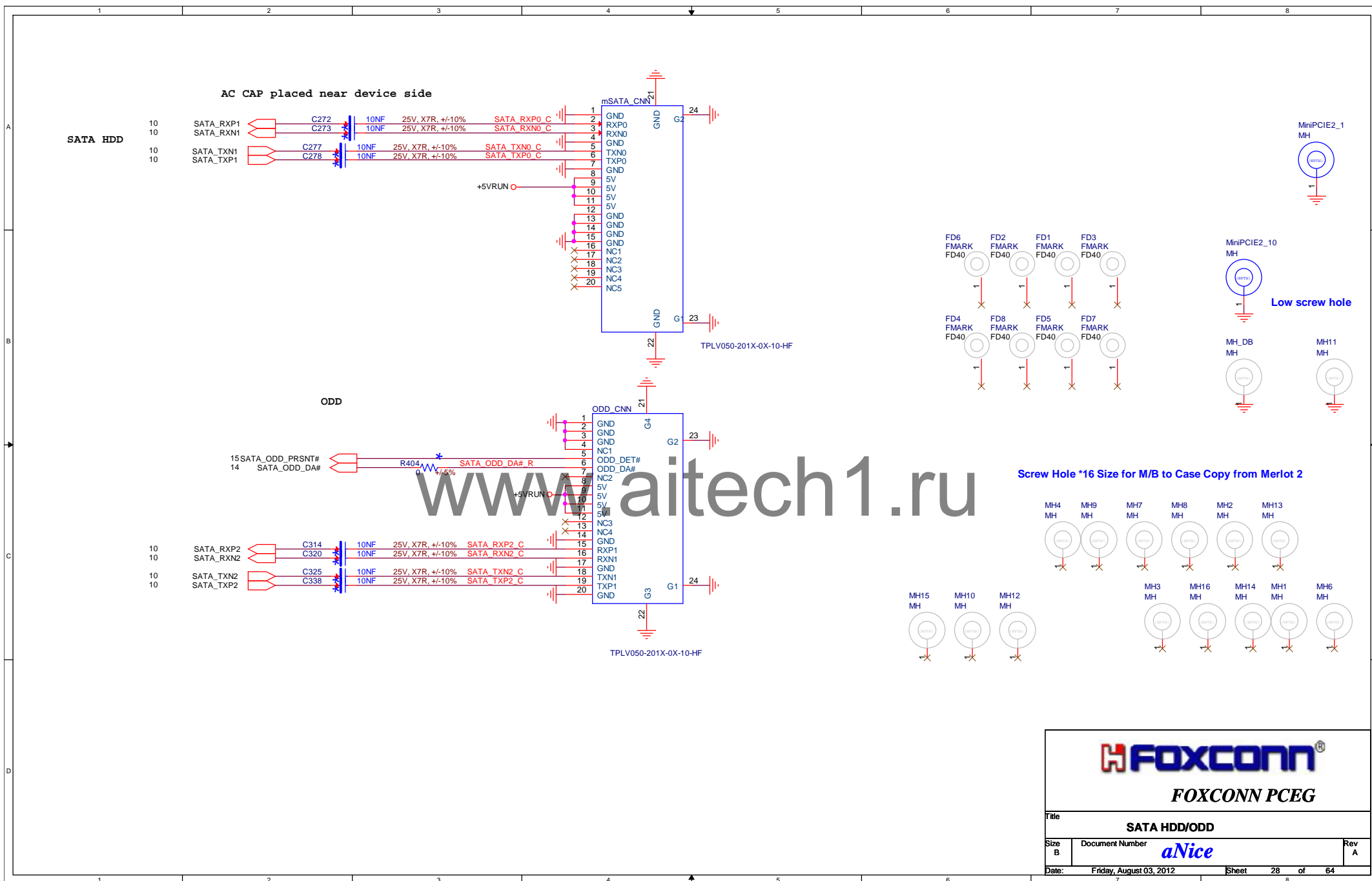
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Title			Audio Speaker(6W)
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The diagram illustrates a 4-bit ripple-carry adder circuit. It consists of four 74VHC14A inverters (U51A, U51B, U51C, U51D, U51E, U51F) and four 74147 decoders (U51A, U51B, U51C, U51D, U51E, U51F). The circuit is powered by +3VALW and +3VALW. The inputs are labeled 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15. The outputs are labeled 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15. The circuit is designed to add two 4-bit numbers and produce a 5-bit result. The inputs are connected to the decoders, and the outputs are connected to the inverters. The ripple-carry mechanism is implemented by connecting the carry-out of one stage to the carry-in of the next stage. The final carry-out is connected to the output of the last stage. The circuit is labeled with '8mil' and '3VALW'.







Touch panel
RC receiver
KB/MS receiver
NFC

PWR_IND indicates the power state from EC. It is used for RF module to decide the key code pass thru USB or STATE_IR. Detail definition will be defined by Suyi and ITE EC team.

+3VALW for proximity
transmitter IR LED power

+EVCC for proximity IC and
OSD touch IC power

+5VAUX for OSD
touch LED power.

OSD & Proximity

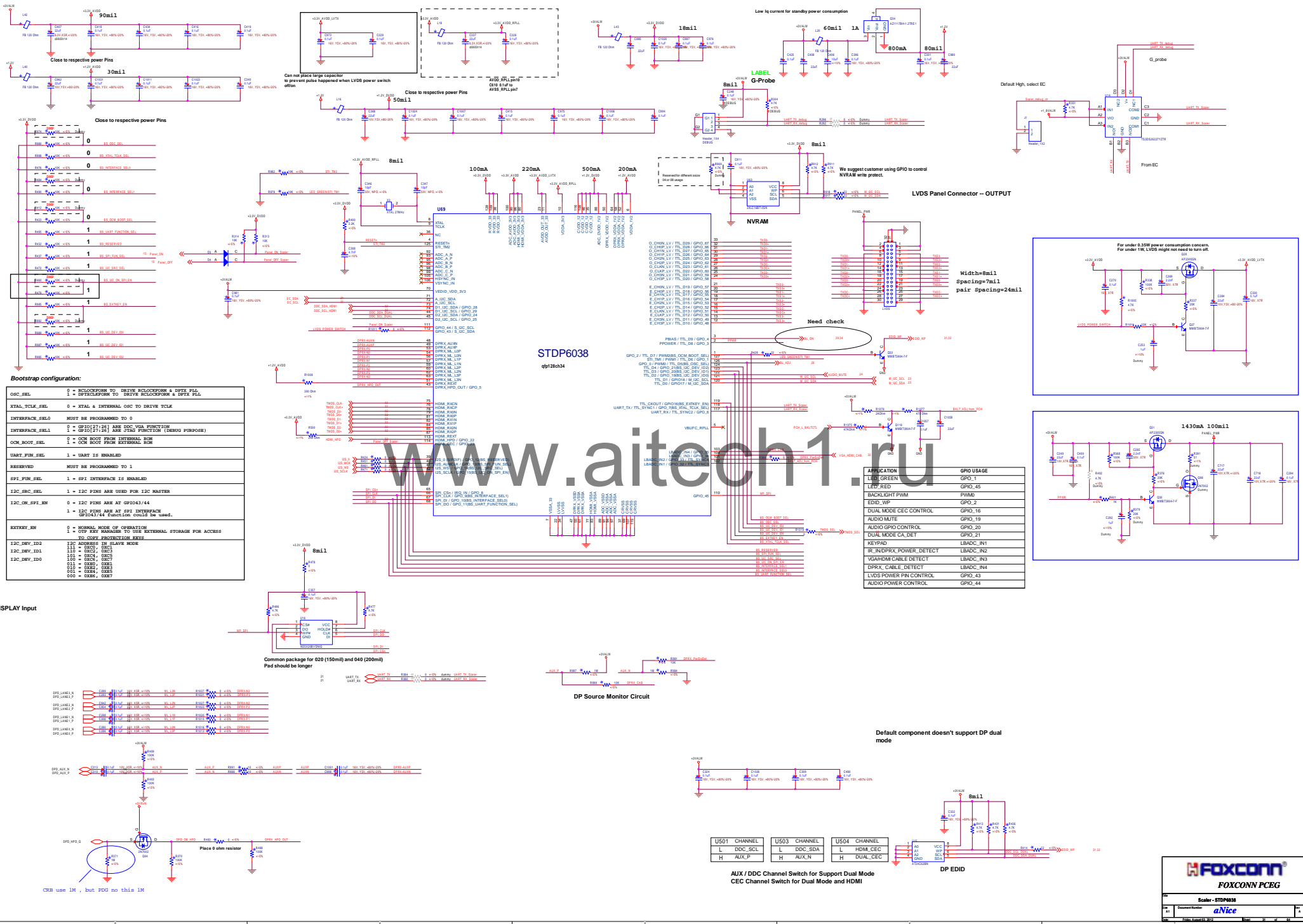
Web cam & Digital MIC

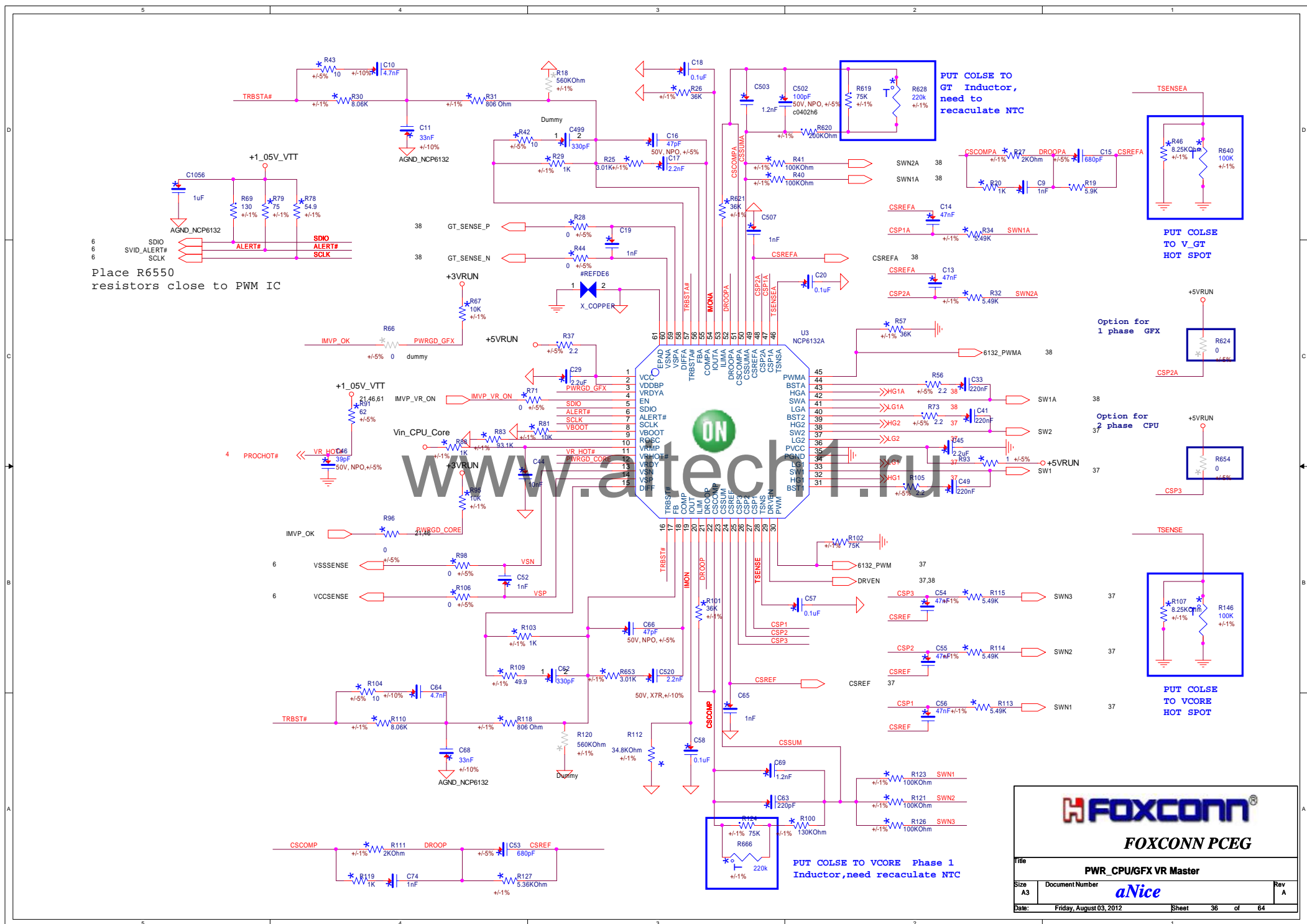
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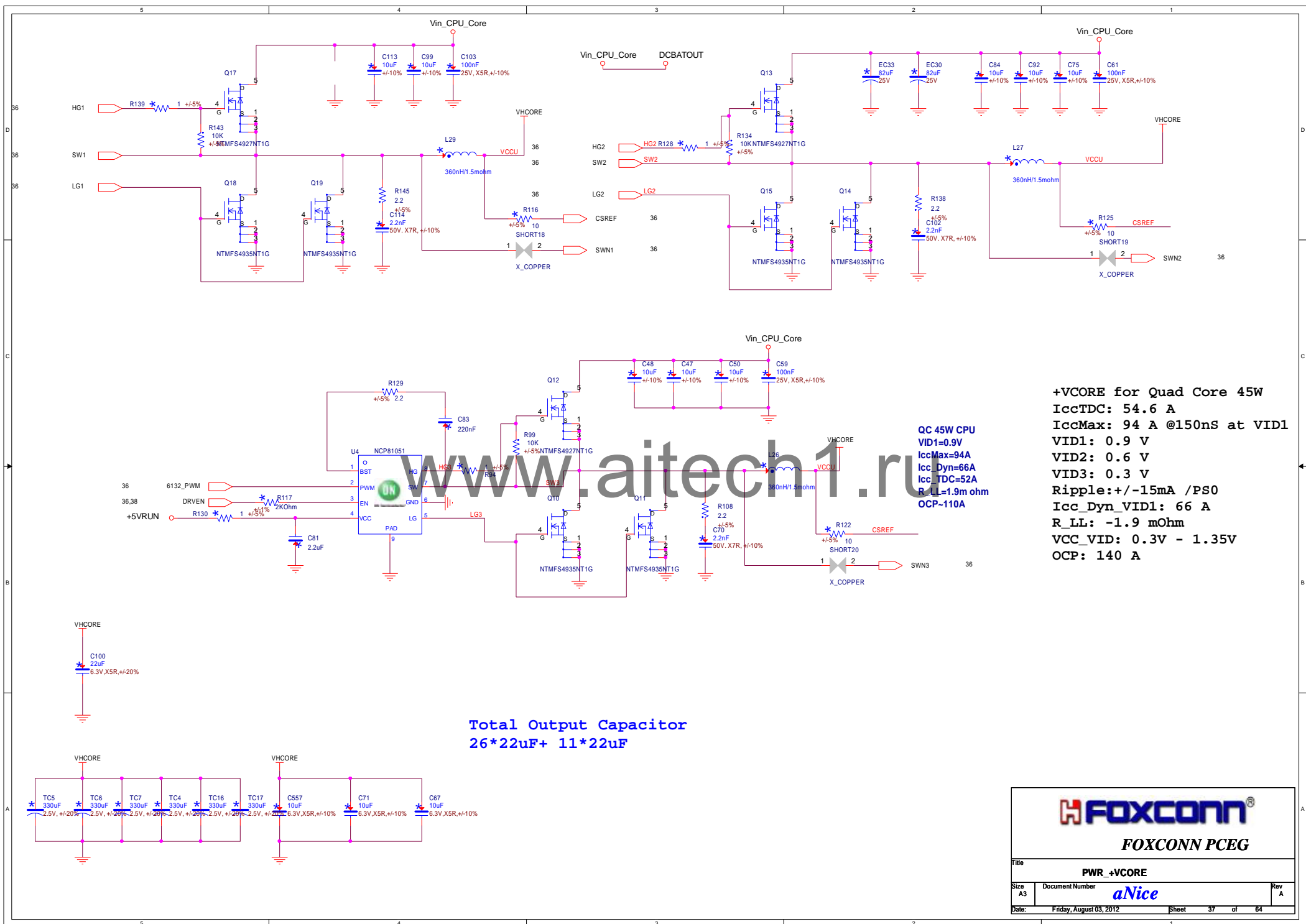
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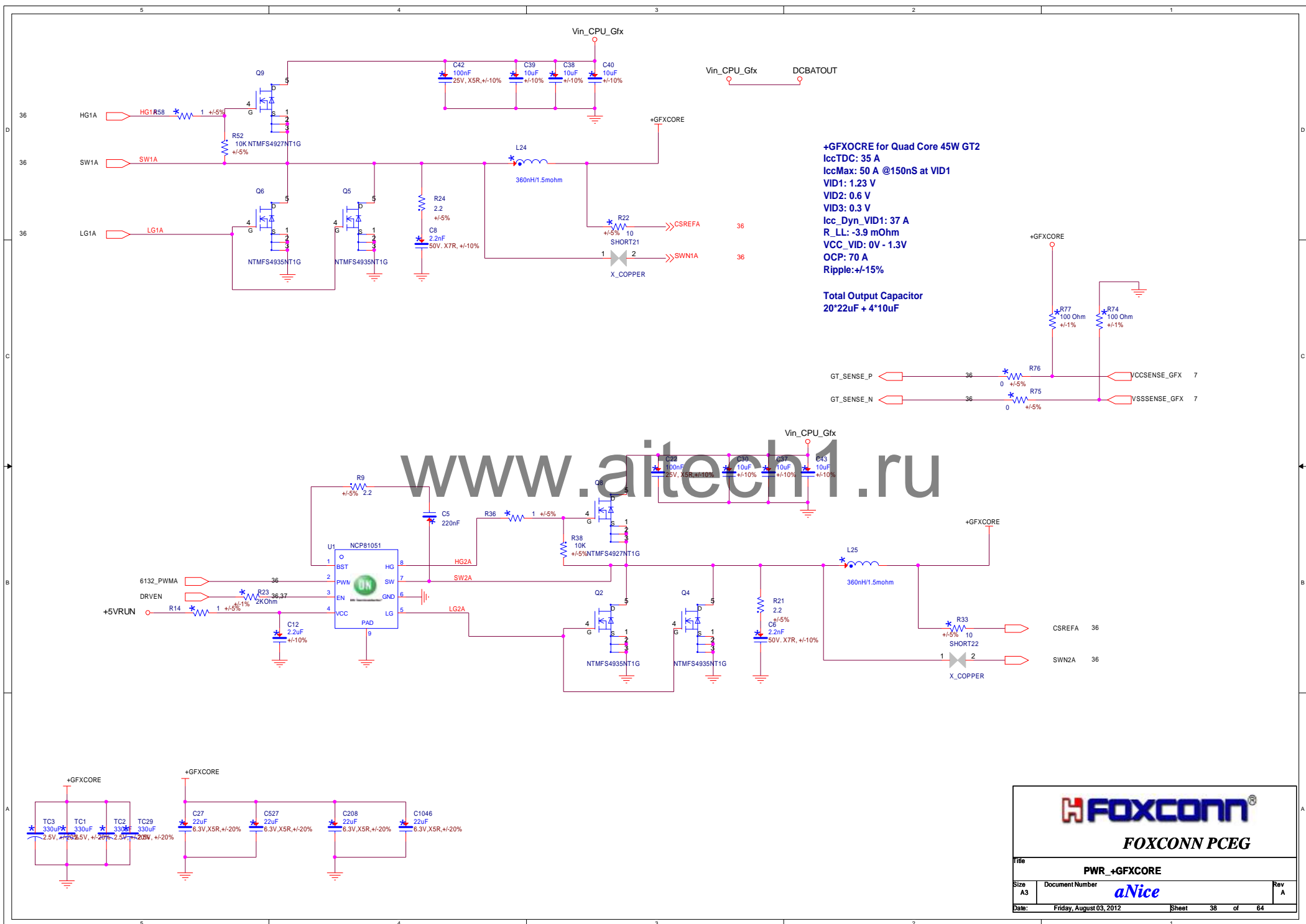
Title			H/W Thermal Protect	
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Title			
PWR_+VCCORE			
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1.05V_PCH&VCCIO

Intel XE & SV

VID0	VID1	Vout
0	0	
0	1	
1	0	
1	1	0.675V

Output Voltage Need to Set to 1.05V Fixed.

VCCIO has 1 select pin from the CPU which MUST be ignored (no connect). The Chief River platform will support a 1.05V VCCIO, and the selection of this voltage must be done on the board. From Doc#458544 PDDG, Page 78

Meet Intel spec.
DC+ripple:±2%
AC:±3%
OCP:23A
Frequency: 300K

VCCIO_CPU 8.5A
+ PCH 6.75A

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1.8V

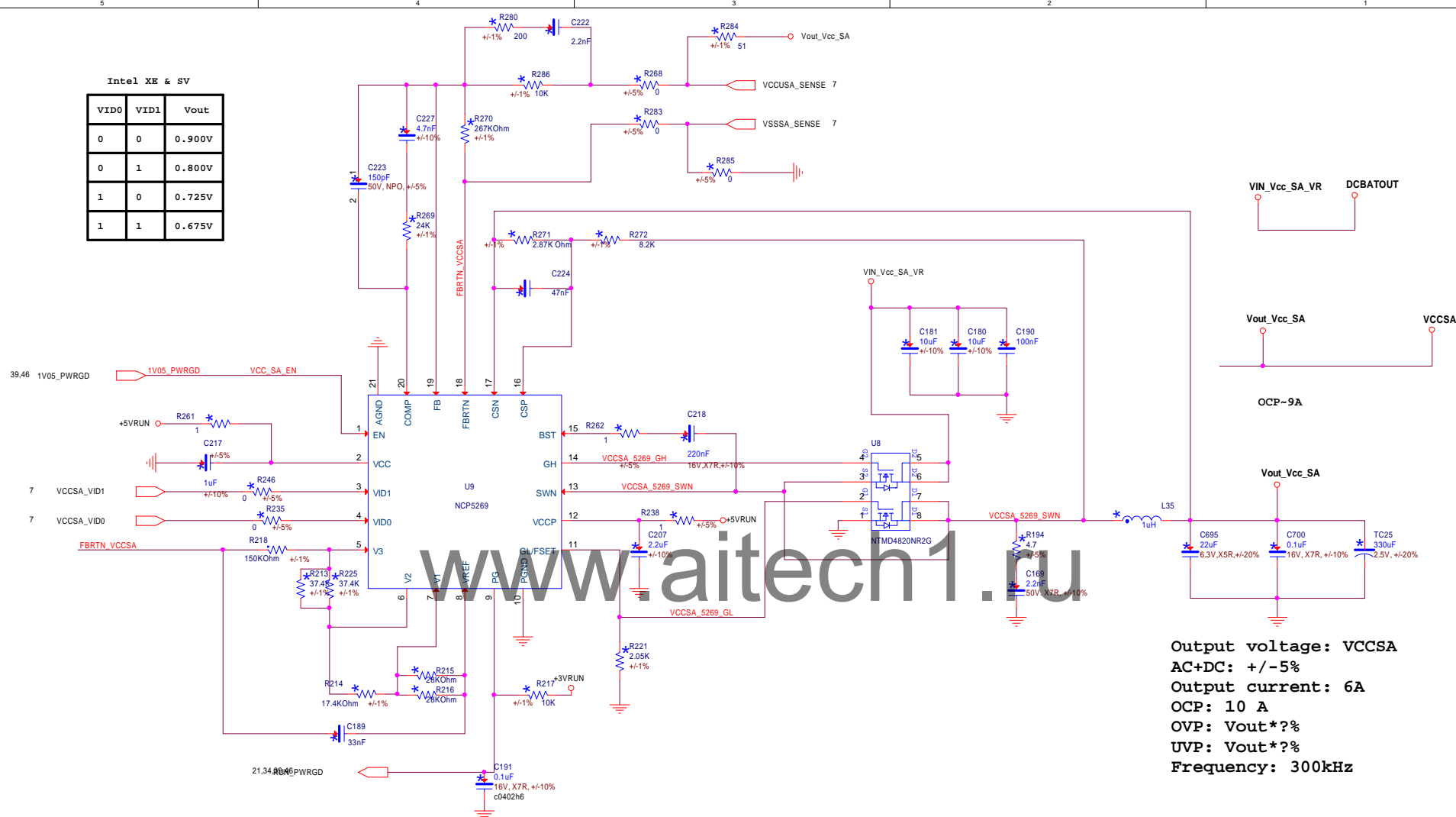
+1.8VRUN ±5%
Thermal Design Current: 1.2A
OCP: ? A

V_1P05_ME

VccASW Imax 0.803A

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FOXCONN PCEG		
File PWR_+1.05V_VTT/+1.8V		
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VID0	VID1	Vout
0	0	0.900V
0	1	0.800V
1	0	0.725V
1	1	0.675V

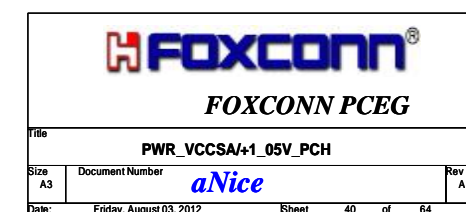


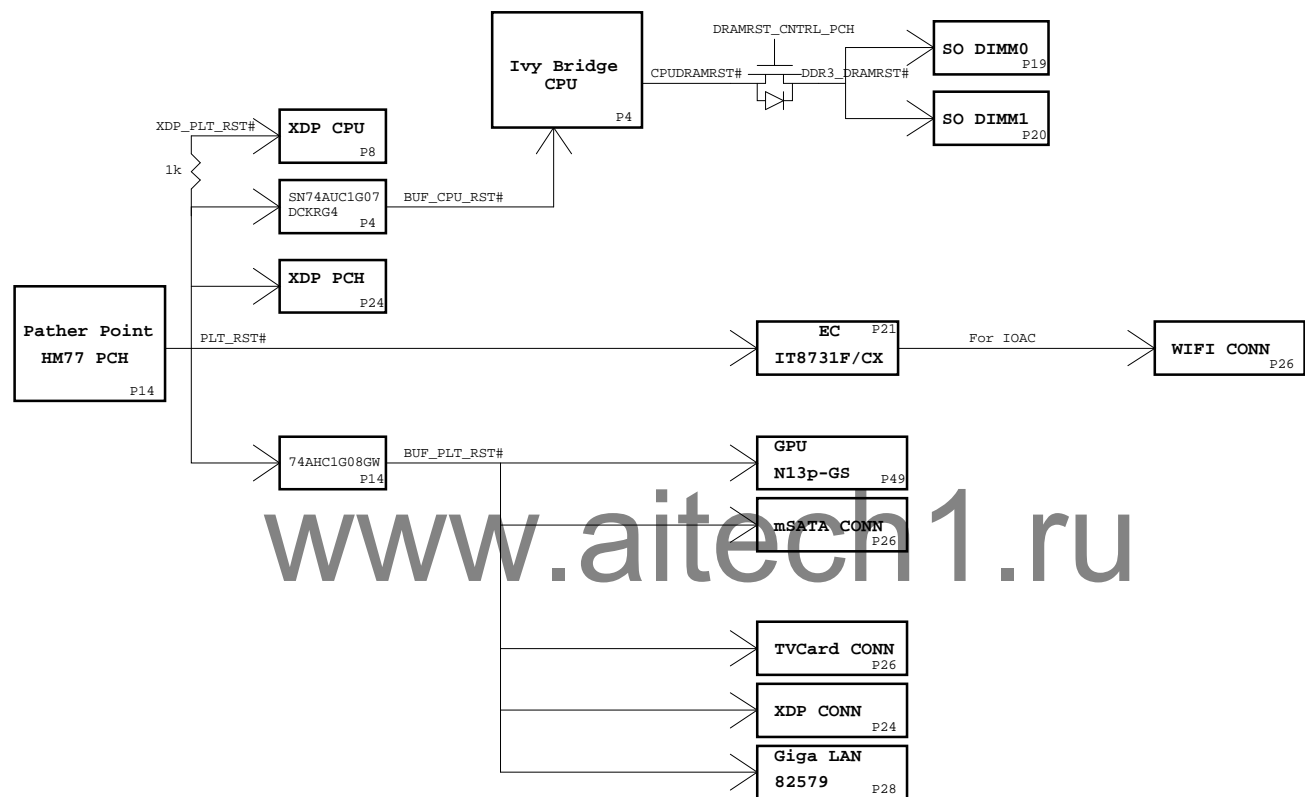
```
Output voltage: VCCSA
AC+DC: +/-5%
Output current: 6A
OCP: 10 A
OVP: Vout*?%
UVP: Vout*?%
Frequency: 300kHz
```

VID control table for VCCSA:

Function	VCCSA_VID0	VCCSA_VID1	Vout
SNB HIGH	0	0	0.9V
IVB HIGH	0	1	0.8V (Mode =open)
	0	1	0.85V (Mode =33k)
SNB LOW	1	0	0.725V
IVB LOW	1	1	0.675V

0.8V for 2011 SV processor and
0.85V for 2011 LV/ULV processor





Audio														Mini PCIE												
	CPU Ivy Bridge	PCH Pather Point	DDR3	GPU N13P-GS /GL	EC IT8731/CX	USB Charger TPS2540RTE	RC Receiver	OSD Touch Panel Proximity	Scaler Board	NFC	Touch Panel	KB/MS Receiver	Camera & Digital Mic	CODEC ALC662	AMP LM48901S	SPDIF/I2C DIR9001PW	I2C/IS2S PCM1754	HDMI PI3VDP411 LSRZBE	mSATA	WIFI	TV Card	Card Reader RTSS5209-GR	LAN 82579	USB2.0 &USB3.0 CONN	SATA &ODD	FAN
S0	VHCORE +GFXCORE VCCSA +1.8VRUN +1.5VSUS	+1.05V_PCH +1.05V_VTT +1.5VRUN +1.8VRUN +3VRUN +5VRUN +5VALW	DDR3_VREF +1.5VSUS +3VRUN	NVVD FBVDD FBVDDQ PEX_VDD PEX_PLVDD 3V3_NV 1V8_NV LVDS_PP	+3VRUN +3VALW +ECVCC	+5VALW	+5VALW	+3VALW +5VALW	+3VALW +5VALW	+5VSUS	+5VSUS	+5VSUS	+3VRUN	+3VRUN +5VSUS	+3VALW +5VALW 1.8VALW	+3VALW	+5VALW	+3VRUN +5VRUN	+3VRUN +1V1_5VRUN	+3VALW +1V1_5VRUN	+3VRUN +1V1_5VRUN	+5VSUS	+3V_LAN	+5VSUS	+5VRUN	+12VRUN
S3	+1.5VSUS	+3VALW +5VALW	+1.5VSUS		+3VALW +ECVCC	+5VALW	+5VALW	+3VALW +5VALW	+3VALW +5VALW	+5VSUS	+5VSUS	+5VSUS		+5VSUS	+3VALW +5VALW 1.8VALW	+3VALW	+5VALW			+3VALW		+5VSUS	+3V_LAN	+5VSUS		
S4/S5 with WOL		+3VALW +5VALW			+3VALW +ECVCC	+5VALW	+5VALW	+3VALW +5VALW	+3VALW +5VALW						+3VALW +5VALW 1.8VALW	+3VALW	+5VALW			+3VALW			+3V_LAN			
S4/S5 without WOL		+3VALW +5VALW			+3VALW +ECVCC	+5VALW	+5VALW	+3VALW +5VALW	+3VALW +5VALW						+3VALW +5VALW 1.8VALW	+3VALW	+5VALW			+3VALW						
EUP6					+ECVCC	+5VALX		+3VALX +5VALX																		



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Title

Device Power Status Table

Size

Document Number

Rev

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Date

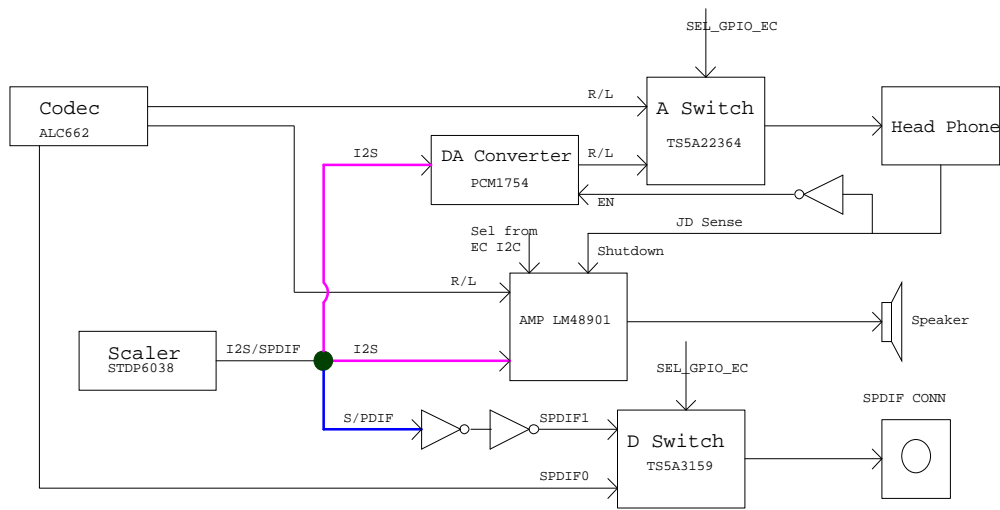
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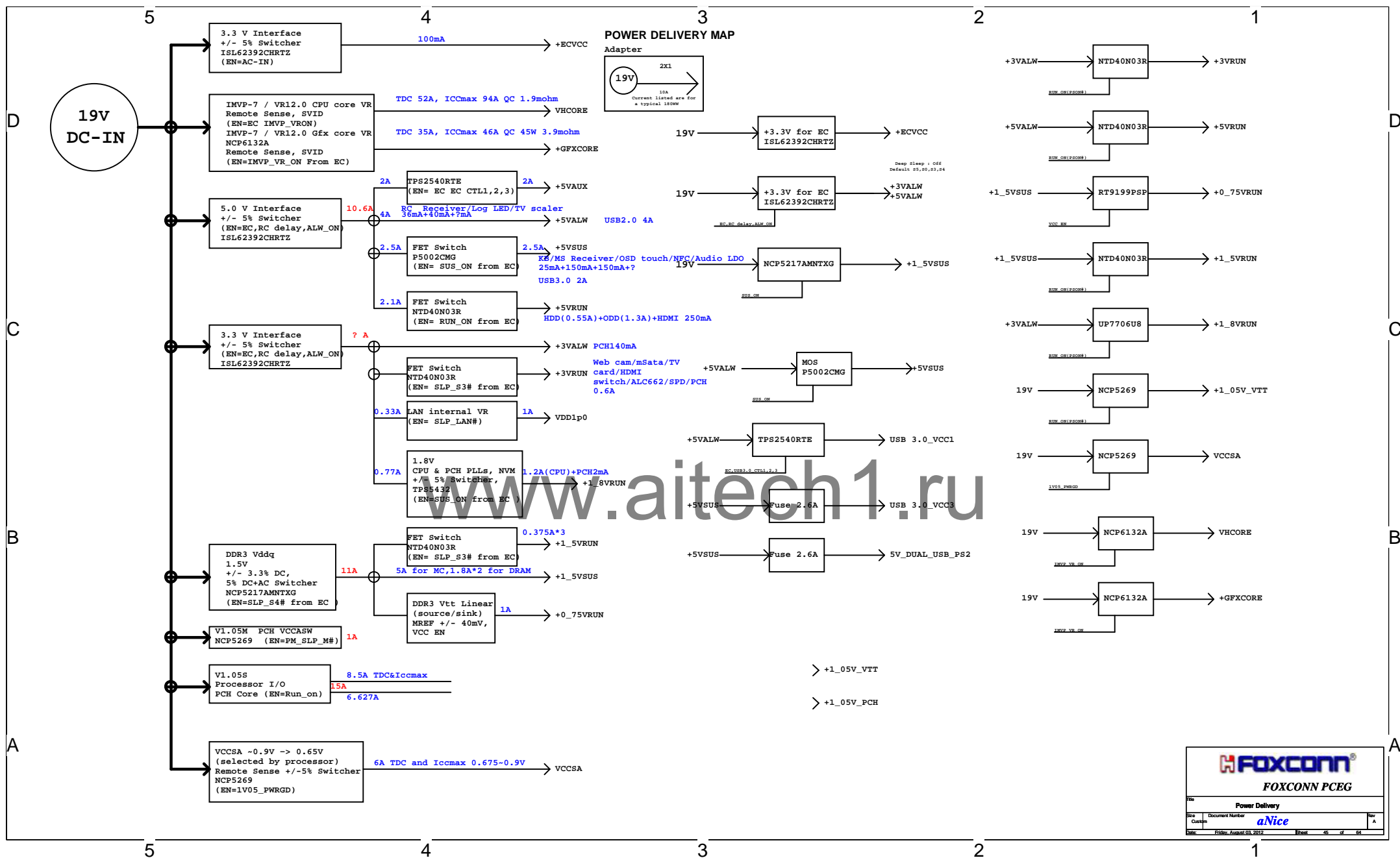
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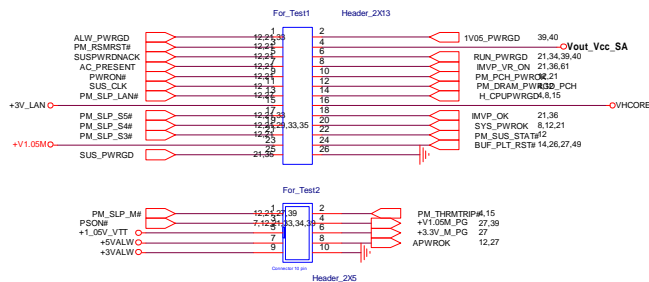
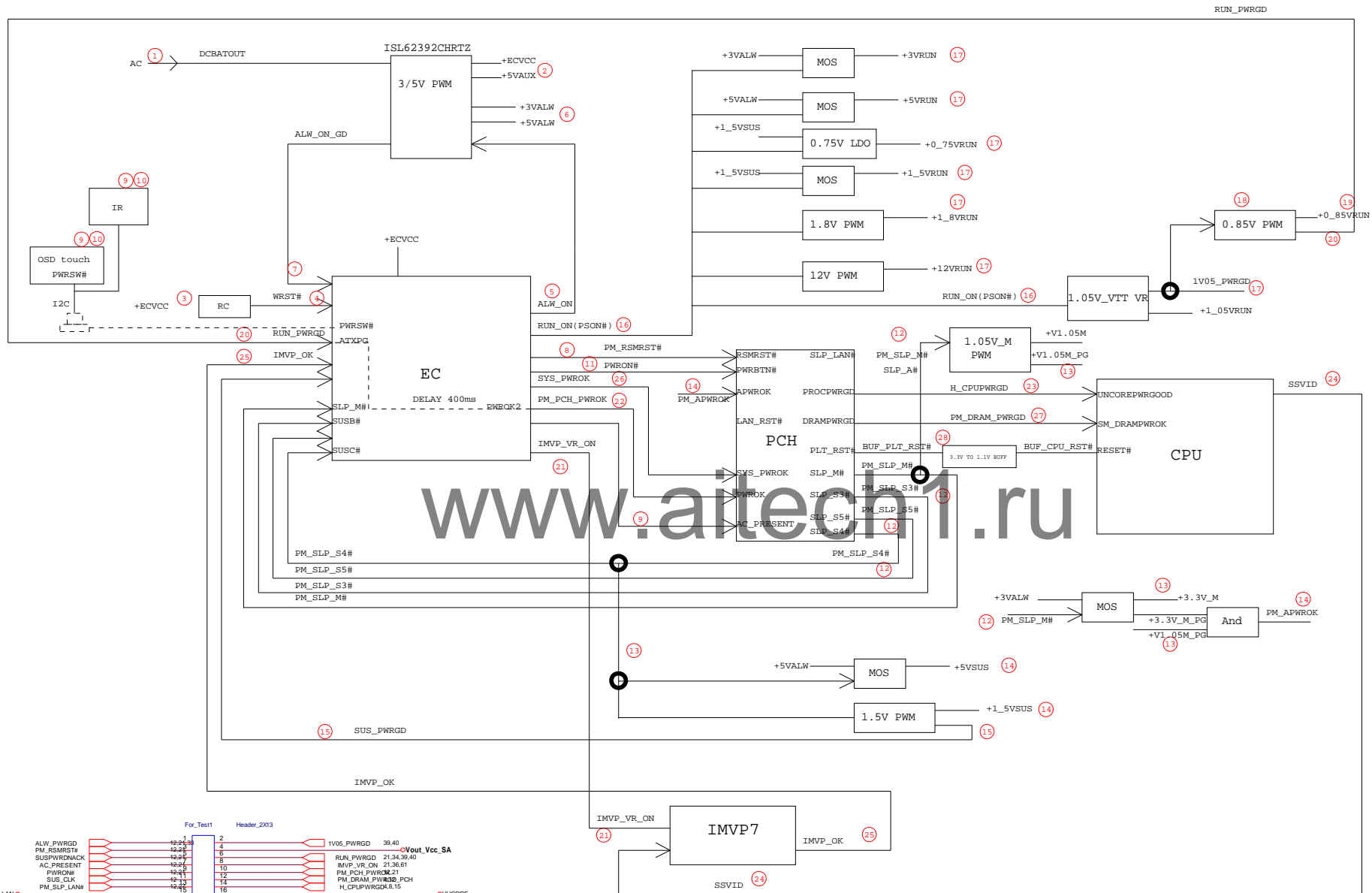
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PC Mode		
Headphone	ON	OFF
Speaker	OFF	ON/OFF
SPDIF	ON/OFF	ON/OFF

HDMI INPUT Mode			
Headphone	ON	OFF	OFF
Speaker	OFF	ON	OFF
SPDIF	OFF	OFF	ON





FOXCONN

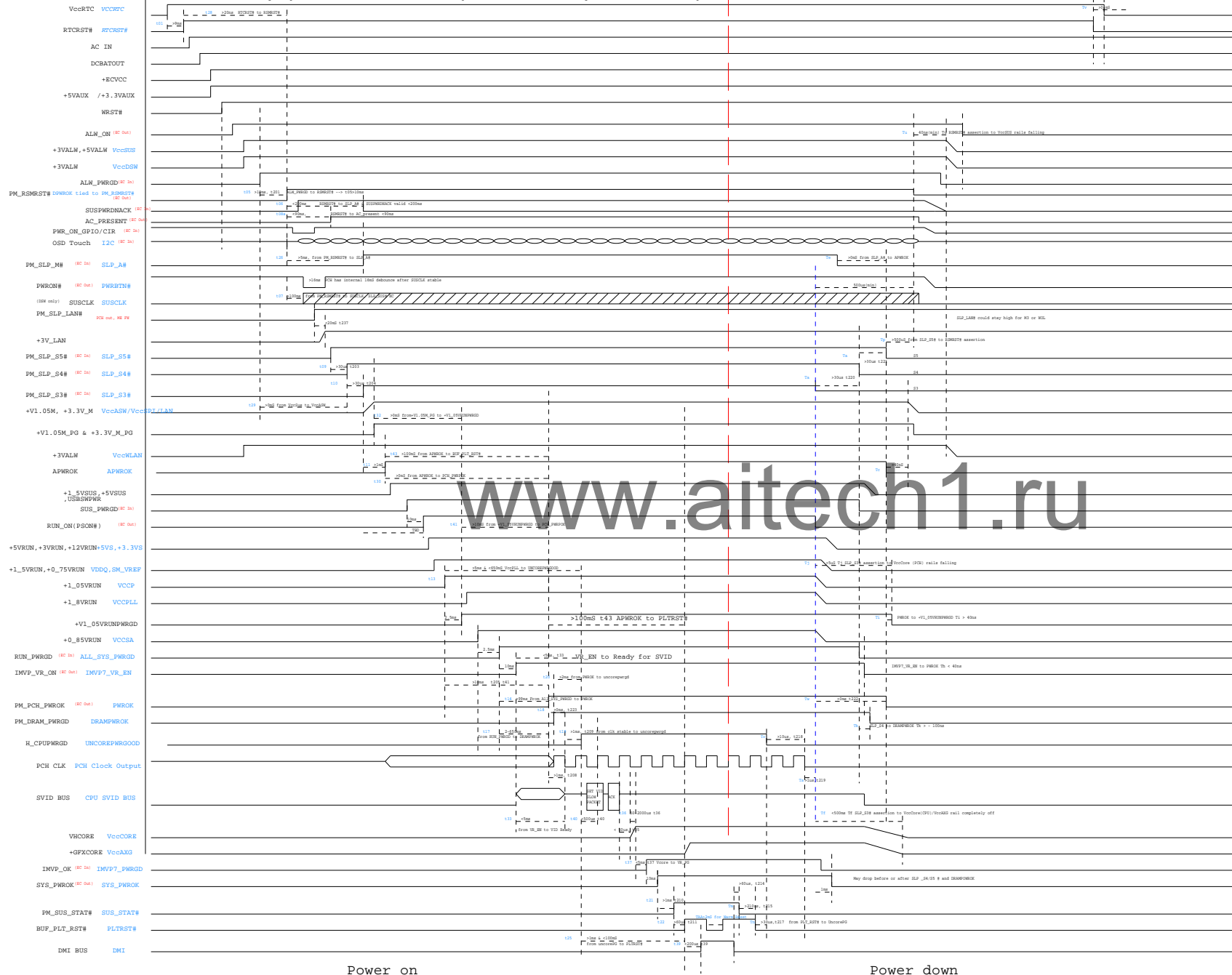
FOXCONN PCEG

File: **POWER SEQUENCE BLOCK**

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Without Deep S4/S5 sequence

The VccRTC will ramp only for the first time after the RTC battery is installed. For the subsequent runs VccRTC will always be ON.



Power on

Power down



POWER SEQUENCE			
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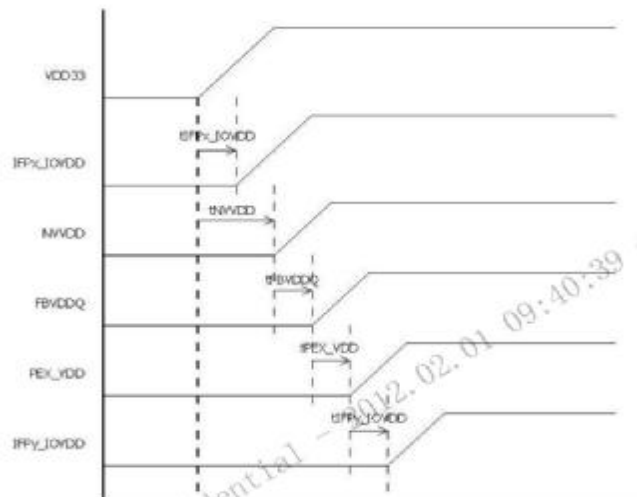


Figure 17. Recommended Power On Sequencing Order

Table 72. DVI Power Rails

Power Rails	Voltage	Max. Current Draw ¹
IFPx_IOVDD (x= E, F)	1.05 V \pm 30 mV	72 mA each
IFPy_PLLVDD (y= EF)	3.3 V \pm 5%	190 mA each

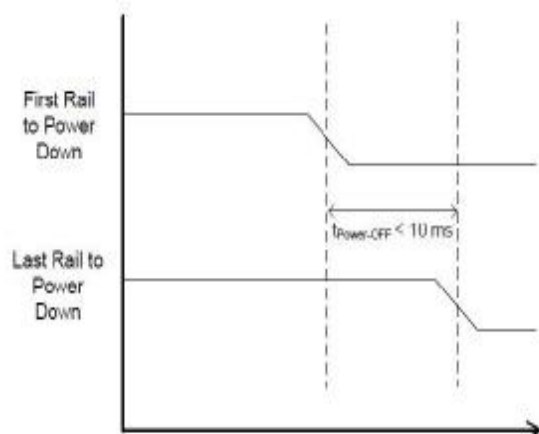


Figure 18. Recommended Power Off Sequencing Order

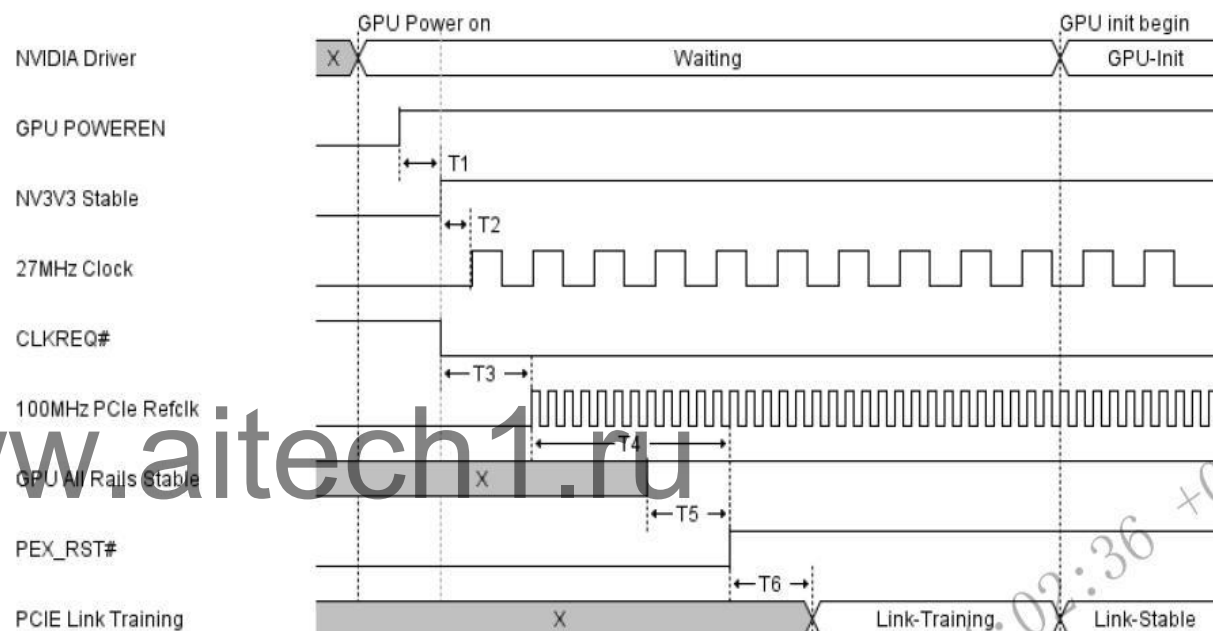


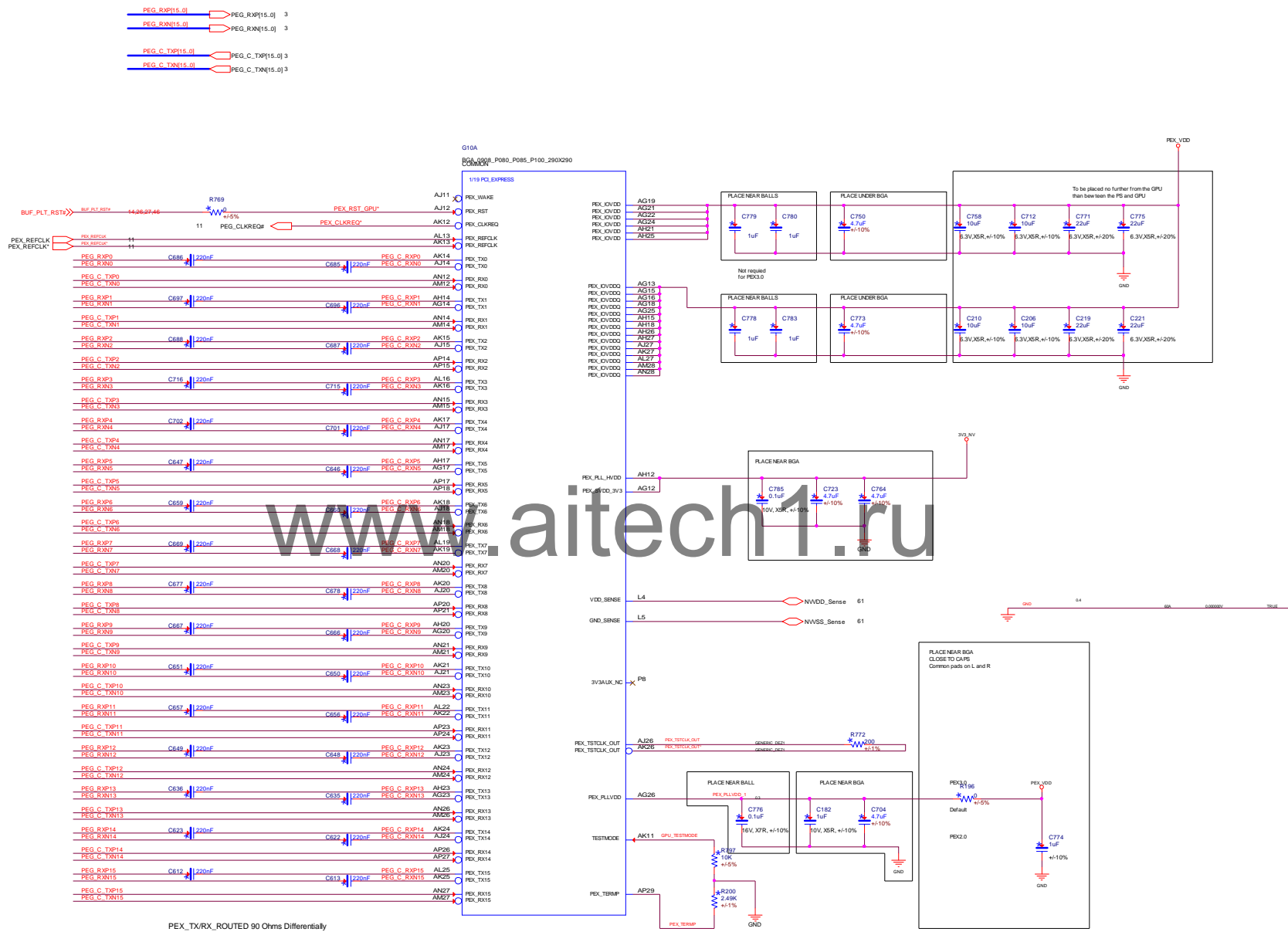
Figure 2. Typical Power-Up Sequence

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FOXCONN PCEG

Title		
GPU Sequence		
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PCI-Express Gen2 x16 Interface

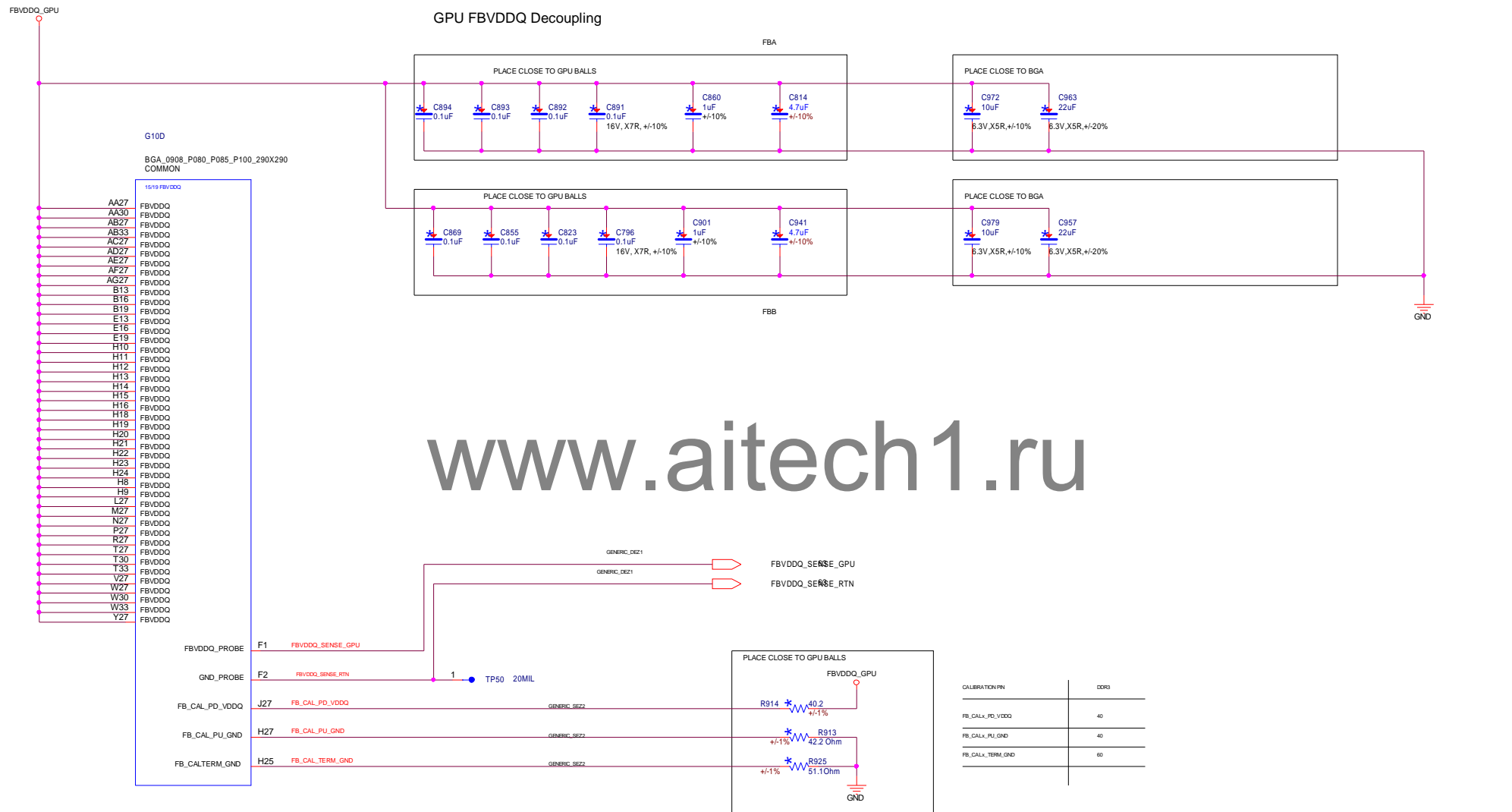


Title		PCIE Gen2 x16 Interface	
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1



Frame Buffer FBVDDQ Power/Decoupling/Calibration



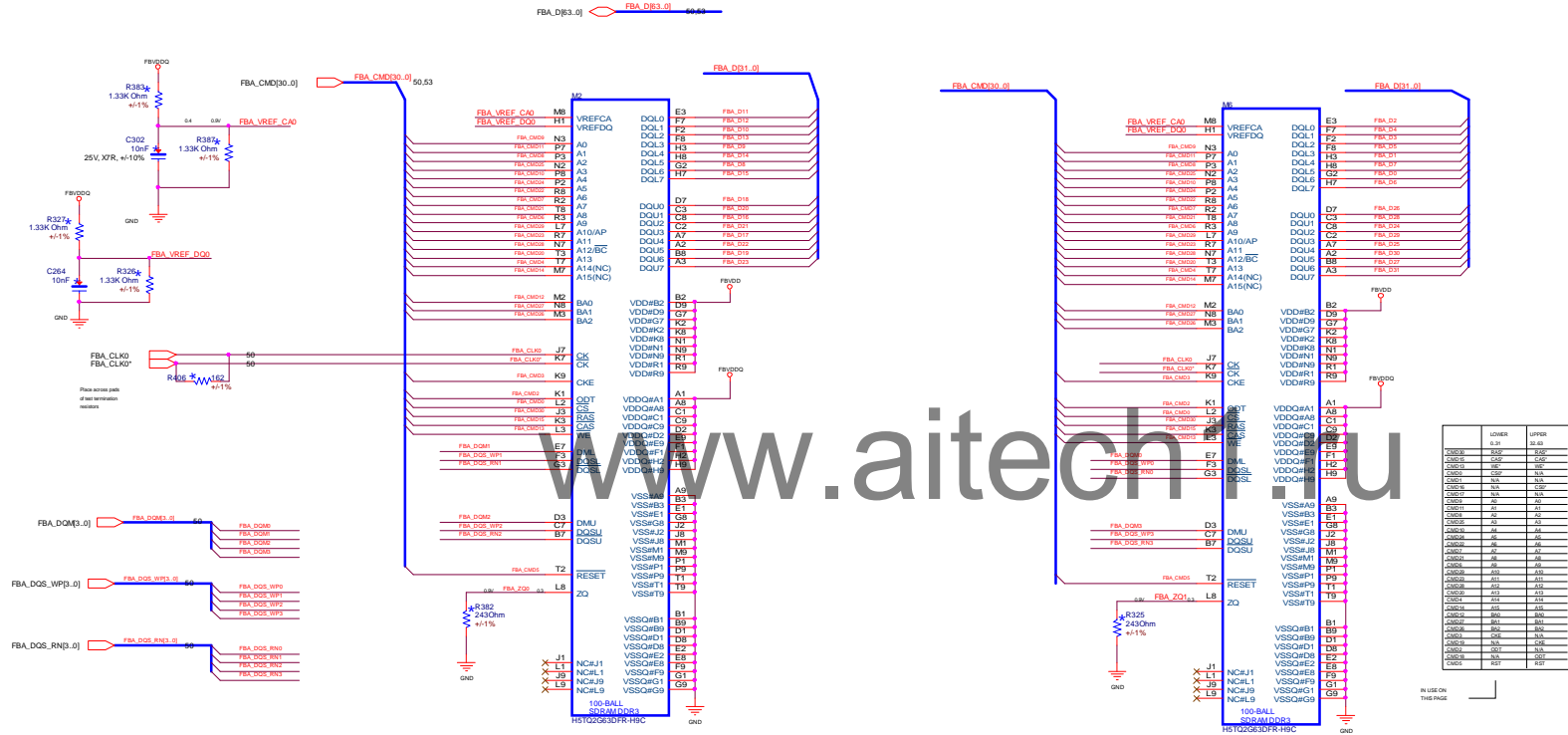
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Frame Buffer FBVDDQ Power/Decoupling/Calibration		
Size	Document Number	Rev
A3	aNice	A
Date: Friday, August 03, 2012 Sheet 51 of 64		

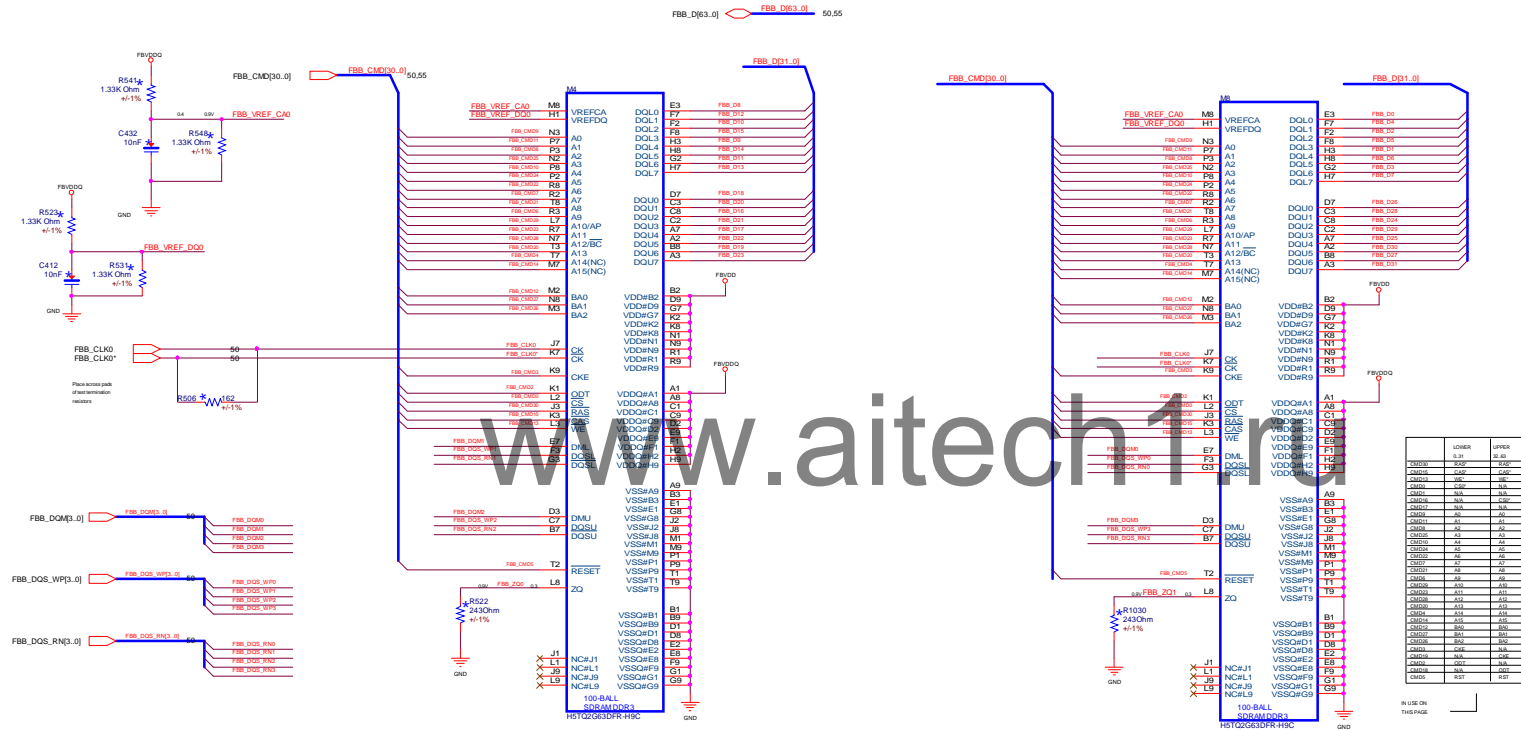
Memory Lower Partition A



	JONER	UPPER
CMD00	0.00	0.00
CMD01	0.00	0.00
CMD02	0.00	0.00
CMD03	0.00	0.00
CMD04	0.00	0.00
CMD05	0.00	0.00
CMD06	0.00	0.00
CMD07	0.00	0.00
CMD08	0.00	0.00
CMD09	0.00	0.00
CMD10	0.00	0.00
CMD11	0.00	0.00
CMD12	0.00	0.00
CMD13	0.00	0.00
CMD14	0.00	0.00
CMD15	0.00	0.00
CMD16	0.00	0.00
CMD17	0.00	0.00
CMD18	0.00	0.00
CMD19	0.00	0.00
CMD20	0.00	0.00
CMD21	0.00	0.00
CMD22	0.00	0.00
CMD23	0.00	0.00
CMD24	0.00	0.00
CMD25	0.00	0.00
CMD26	0.00	0.00
CMD27	0.00	0.00
CMD28	0.00	0.00
CMD29	0.00	0.00
CMD30	0.00	0.00
CMD31	0.00	0.00
CMD32	0.00	0.00
CMD33	0.00	0.00
CMD34	0.00	0.00
CMD35	0.00	0.00
CMD36	0.00	0.00
CMD37	0.00	0.00
CMD38	0.00	0.00
CMD39	0.00	0.00
CMD40	0.00	0.00
CMD41	0.00	0.00
CMD42	0.00	0.00
CMD43	0.00	0.00
CMD44	0.00	0.00
CMD45	0.00	0.00
CMD46	0.00	0.00
CMD47	0.00	0.00
CMD48	0.00	0.00
CMD49	0.00	0.00
CMD50	0.00	0.00
CMD51	0.00	0.00
CMD52	0.00	0.00
CMD53	0.00	0.00
CMD54	0.00	0.00
CMD55	0.00	0.00
CMD56	0.00	0.00
CMD57	0.00	0.00
CMD58	0.00	0.00
CMD59	0.00	0.00
CMD60	0.00	0.00
CMD61	0.00	0.00
CMD62	0.00	0.00
CMD63	0.00	0.00
CMD64	0.00	0.00
CMD65	0.00	0.00
CMD66	0.00	0.00
CMD67	0.00	0.00
CMD68	0.00	0.00
CMD69	0.00	0.00
CMD70	0.00	0.00
CMD71	0.00	0.00
CMD72	0.00	0.00
CMD73	0.00	0.00
CMD74	0.00	0.00
CMD75	0.00	0.00
CMD76	0.00	0.00
CMD77	0.00	0.00
CMD78	0.00	0.00
CMD79	0.00	0.00
CMD80	0.00	0.00
CMD81	0.00	0.00
CMD82	0.00	0.00
CMD83	0.00	0.00
CMD84	0.00	0.00
CMD85	0.00	0.00
CMD86	0.00	0.00
CMD87	0.00	0.00
CMD88	0.00	0.00
CMD89	0.00	0.00
CMD90	0.00	0.00
CMD91	0.00	0.00
CMD92	0.00	0.00
CMD93	0.00	0.00
CMD94	0.00	0.00
CMD95	0.00	0.00
CMD96	0.00	0.00
CMD97	0.00	0.00
CMD98	0.00	0.00
CMD99	0.00	0.00
CMD100	0.00	0.00

```
FBA_CLK/* 80DEZ
FBA_DQS_WP/RN 80DEZ
FBA_DQ/M_WP/RN 45SEZ
FBA_CMD 45SEZ
```

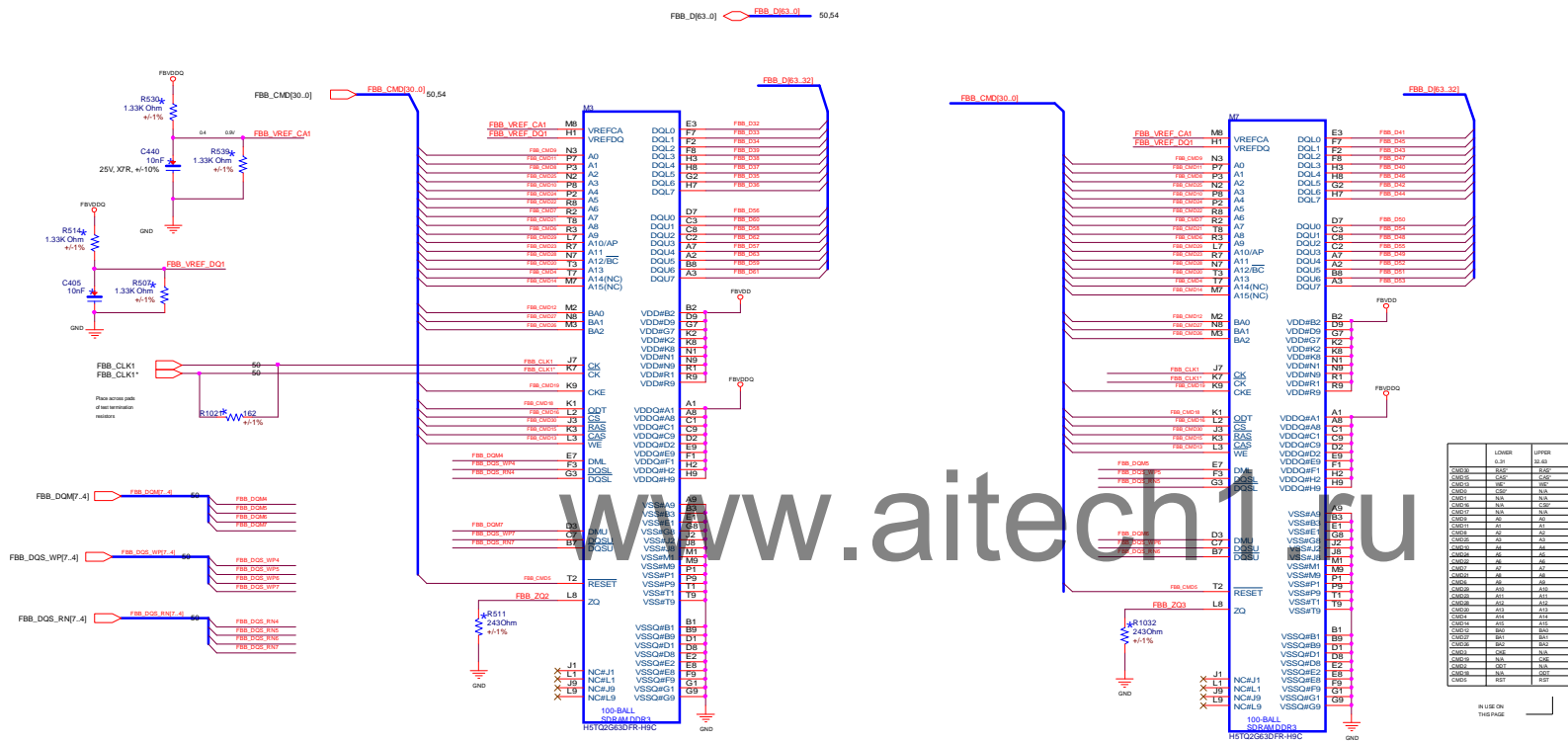

Memory Lower Partition B



	LOWER SE 49	UPPER SE 49
CM0000	E-02	E-02
CM0005	C-05	C-05
CM0010	D-10	D-10
CM0015	D-15	D-15
CM0020	D-20	D-20
CM0025	D-25	D-25
CM0030	D-30	D-30
CM0035	D-35	D-35
CM0040	D-40	D-40
CM0045	D-45	D-45
CM0050	D-50	D-50
CM0055	D-55	D-55
CM0060	D-60	D-60
CM0065	D-65	D-65
CM0070	D-70	D-70
CM0075	D-75	D-75
CM0080	D-80	D-80
CM0085	D-85	D-85
CM0090	D-90	D-90
CM0095	D-95	D-95
CM0100	D-100	D-100
CM0105	D-105	D-105
CM0110	D-110	D-110
CM0115	D-115	D-115
CM0120	D-120	D-120
CM0125	D-125	D-125
CM0130	D-130	D-130
CM0135	D-135	D-135
CM0140	D-140	D-140
CM0145	D-145	D-145
CM0150	D-150	D-150
CM0155	D-155	D-155
CM0160	D-160	D-160
CM0165	D-165	D-165
CM0170	D-170	D-170
CM0175	D-175	D-175
CM0180	D-180	D-180
CM0185	D-185	D-185
CM0190	D-190	D-190
CM0195	D-195	D-195
CM0200	D-200	D-200
CM0205	D-205	D-205
CM0210	D-210	D-210
CM0215	D-215	D-215
CM0220	D-220	D-220
CM0225	D-225	D-225
CM0230	D-230	D-230
CM0235	D-235	D-235
CM0240	D-240	D-240
CM0245	D-245	D-245
CM0250	D-250	D-250
CM0255	D-255	D-255
CM0260	D-260	D-260
CM0265	D-265	D-265
CM0270	D-270	D-270
CM0275	D-275	D-275
CM0280	D-280	D-280
CM0285	D-285	D-285
CM0290	D-290	D-290
CM0295	D-295	D-295
CM0300	D-300	D-300
CM0305	D-305	D-305
CM0310	D-310	D-310
CM0315	D-315	D-315
CM0320	D-320	D-320
CM0325	D-325	D-325
CM0330	D-330	D-330
CM0335	D-335	D-335
CM0340	D-340	D-340
CM0345	D-345	D-345
CM0350	D-350	D-350
CM0355	D-355	D-355
CM0360	D-360	D-360
CM0365	D-365	D-365
CM0370	D-370	D-370
CM0375	D-375	D-375
CM0380	D-380	D-380
CM0385	D-385	D-385
CM0390	D-390	D-390
CM0395	D-395	D-395

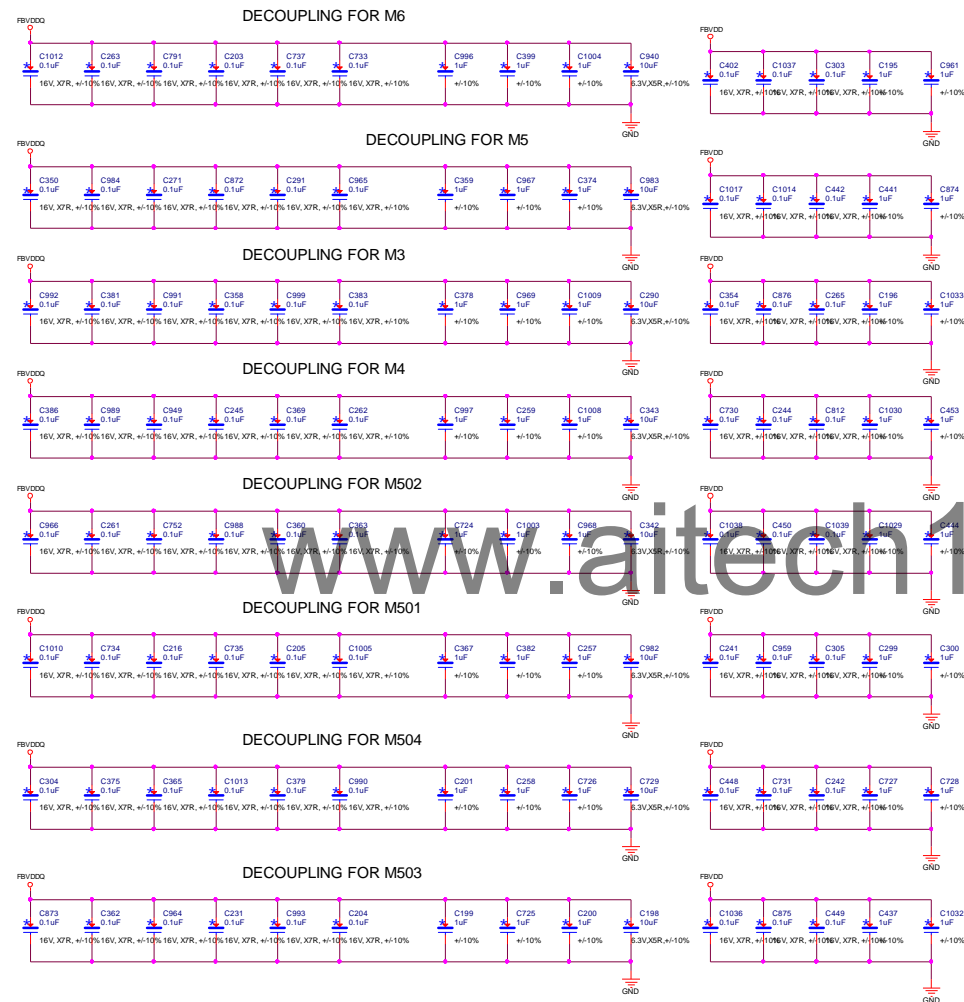
```
FBA_CLK/* 80DEZ
FBA_DQS_WP/RN 80DEZ
FBA_DQ/M_WP/RN 45SEZ
FBA_CMD 45SEZ
```

Memory Upper Partition B



	LOWER	UPPER
CMB0	B12	B12
CMB1	B12	C45
CMB2	C45	B12
CMB3	C45	B12
CMB4	B12	C45
CMB5	B12	C45
CMB6	B12	C45
CMB7	B12	B12
CMB8	B12	B12
CMB9	B12	B12
CMB10	B12	B12
CMB11	B12	B12
CMB12	B12	B12
CMB13	B12	B12
CMB14	B12	B12
CMB15	B12	B12
CMB16	B12	B12
CMB17	B12	B12
CMB18	B12	B12
CMB19	B12	B12
CMB20	B12	B12
CMB21	B12	B12
CMB22	B12	B12
CMB23	B12	B12
CMB24	B12	B12
CMB25	B12	B12
CMB26	B12	B12
CMB27	B12	B12
CMB28	B12	B12
CMB29	B12	B12
CMB30	B12	B12
CMB31	B12	B12
CMB32	B12	B12
CMB33	B12	B12
CMB34	B12	B12
CMB35	B12	B12
CMB36	B12	B12
CMB37	B12	B12
CMB38	B12	B12
CMB39	B12	B12
CMB40	B12	B12
CMB41	B12	B12
CMB42	B12	B12
CMB43	B12	B12
CMB44	B12	B12
CMB45	B12	B12
CMB46	B12	B12
CMB47	B12	B12
CMB48	B12	B12
CMB49	B12	B12
CMB50	B12	B12
CMB51	B12	B12
CMB52	B12	B12
CMB53	B12	B12
CMB54	B12	B12
CMB55	B12	B12
CMB56	B12	B12
CMB57	B12	B12
CMB58	B12	B12
CMB59	B12	B12
CMB60	B12	B12
CMB61	B12	B12
CMB62	B12	B12
CMB63	B12	B12
CMB64	B12	B12
CMB65	B12	B12
CMB66	B12	B12
CMB67	B12	B12
CMB68	B12	B12
CMB69	B12	B12
CMB70	B12	B12
CMB71	B12	B12
CMB72	B12	B12
CMB73	B12	B12
CMB74	B12	B12
CMB75	B12	B12
CMB76	B12	B12
CMB77	B12	B12
CMB78	B12	B12
CMB79	B12	B12
CMB80	B12	B12
CMB81	B12	B12
CMB82	B12	B12
CMB83	B12	B12
CMB84	B12	B12
CMB85	B12	B12
CMB86	B12	B12
CMB87	B12	B12
CMB88	B12	B12
CMB89	B12	B12
CMB90	B12	B12
CMB91	B12	B12
CMB92	B12	B12
CMB93	B12	B12
CMB94	B12	B12
CMB95	B12	B12
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CMB97	B12	B12
CMB98	B12	B12
CMB99	B12	B12
CMB100	B12	B12

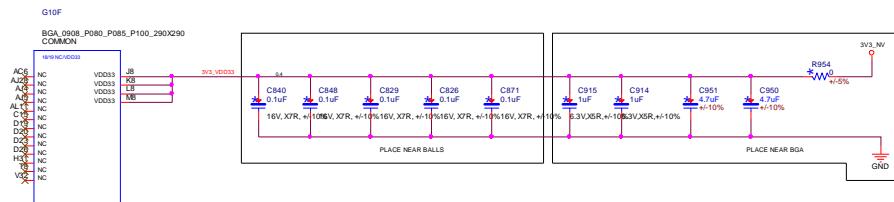
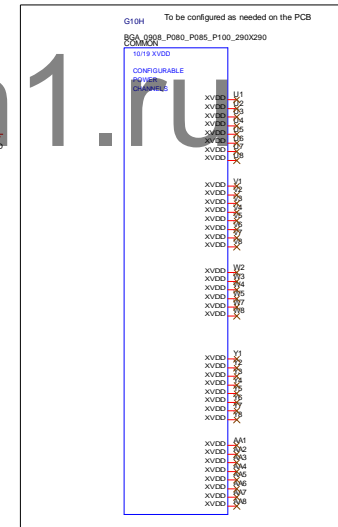
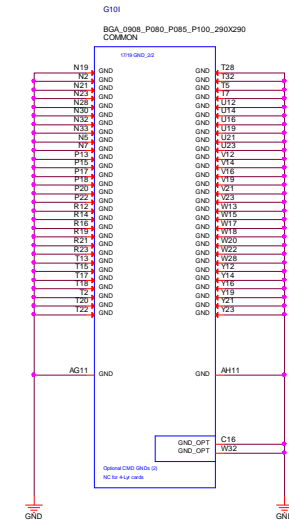
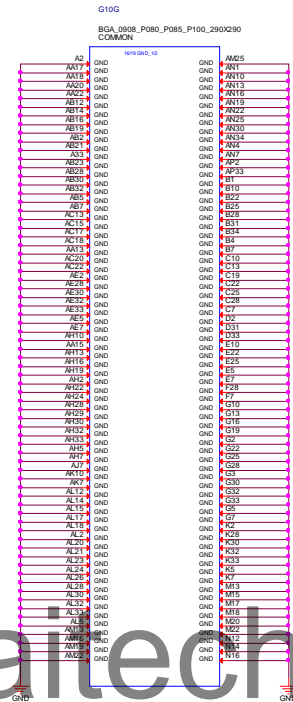
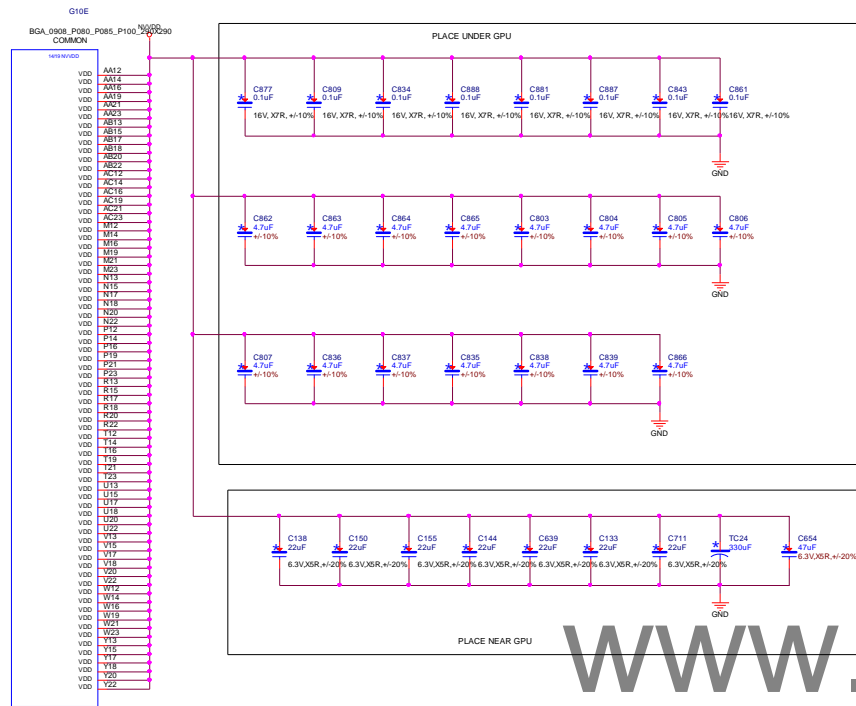
Memory FBVDD/Q Decoupling



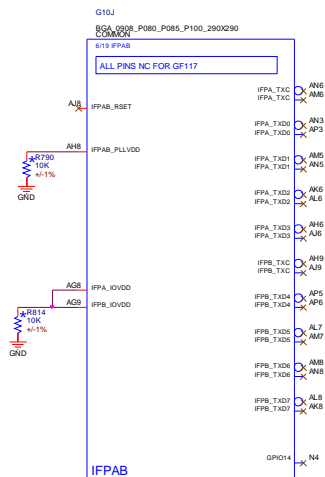
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Memory FBVDD/Q Decoupling			
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Date	Friday, August 03, 2012	Sheet	58 of 64

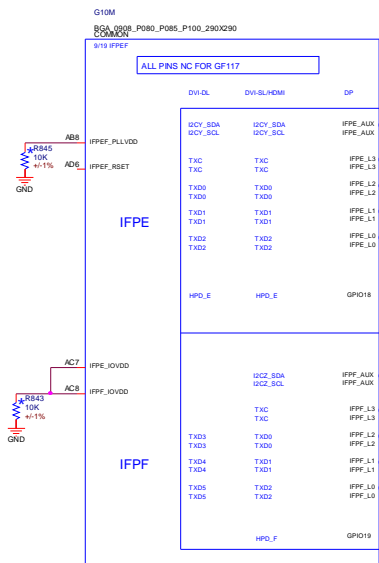
Power/Decoupling: NVVDD,3V3_NV,GRND,and Optional



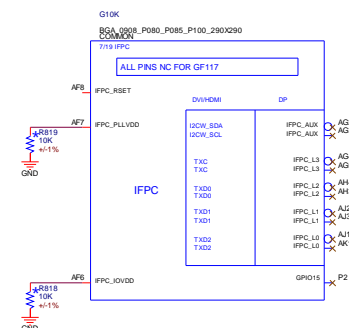
IFPA/B LVDS Dual Link



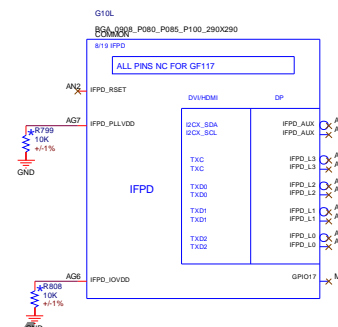
IFPE/F Dual Link TMDS DVI-I



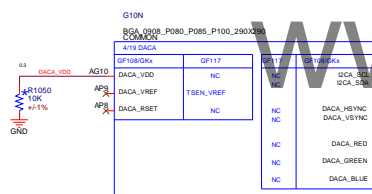
IFPC NATIVE HDMI OR DP




IFPD DUAL MODE DP



DAC_A VGA



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Title				
GPU I/O				
Size	Document Number			Rev
Custom	aNice			
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The schematic diagram illustrates the DP1 debug port circuit. Key components and connections include:

- PEX_VDD Section:** Features a resistor R297 (FB 30 Ohm) and a capacitor C811 (1uF) connected to PEX_VDD. A note indicates "Place Close to GPU".
- GPU_PLLVDD Section:** Includes a capacitor C818 (22uF) connected to GPU_PLLVDD. A note indicates "Place Close to GPU".
- XTAL Section:** Shows the XTALIN and XTALOUT pins connected to a crystal (XTAL 27MHz) and a buffer (XTALOUTBUFF). A note indicates "STUFF PDS on XTALSSIN and XTALOUTBUFF WHEN EXT_SS IS NOT USED".
- Debug Port Mapping:** A table titled "Debug Port_1 Mapping" shows the connection between the DP1 debug port pins and the target device pins. The table is as follows:

Debug Port_1	Source
DP1_0	TP72_3
DP1_1	TP74_5
DP1_2	TP75_5
DP1_3	TP76_5
DP1_4	TP77_5
DP1_5	TP78_5
DP1_6	TP79_5

MECHANICAL COMPONENTS

```

Debug\4 Source
DELG_PORT132 570:4A9
DELG_PORT133 570:4A9
DELG_PORT134 570:4A9
DELG_PORT135 570:4A9
DELG_PORT136 570:4A9
DELG_PORT137 570:4A9
DELG_PORT138 570:4A9
DELG_PORT139 570:4A9
DELG_PORT140 570:4A9

```

GF117/GK10X STRAPPING MODE TABLE			
PIN NAME	MULTI-LEVEL	BINARY PRODUCTION	BINARY BRINGUP
MULTI_STRAP_REF_GND	40.2K TO GND	NOT SUPPORTED	NO STUFF

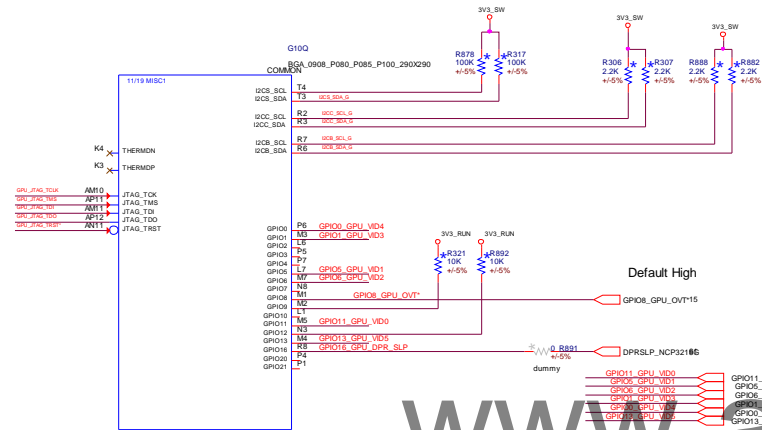
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GPIOs, Thermal Sensor, I2C/GPIO Expanders

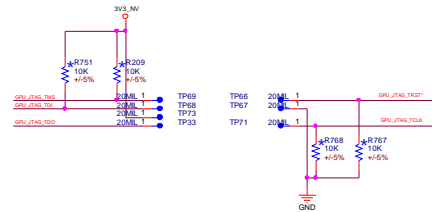
TEMP SENSOR

Route THERMADAC at 0.125mm spacing
with 0.125mm grid guard traces

Place close to GPU near
normal disc hole



JTAG CONNECTOR



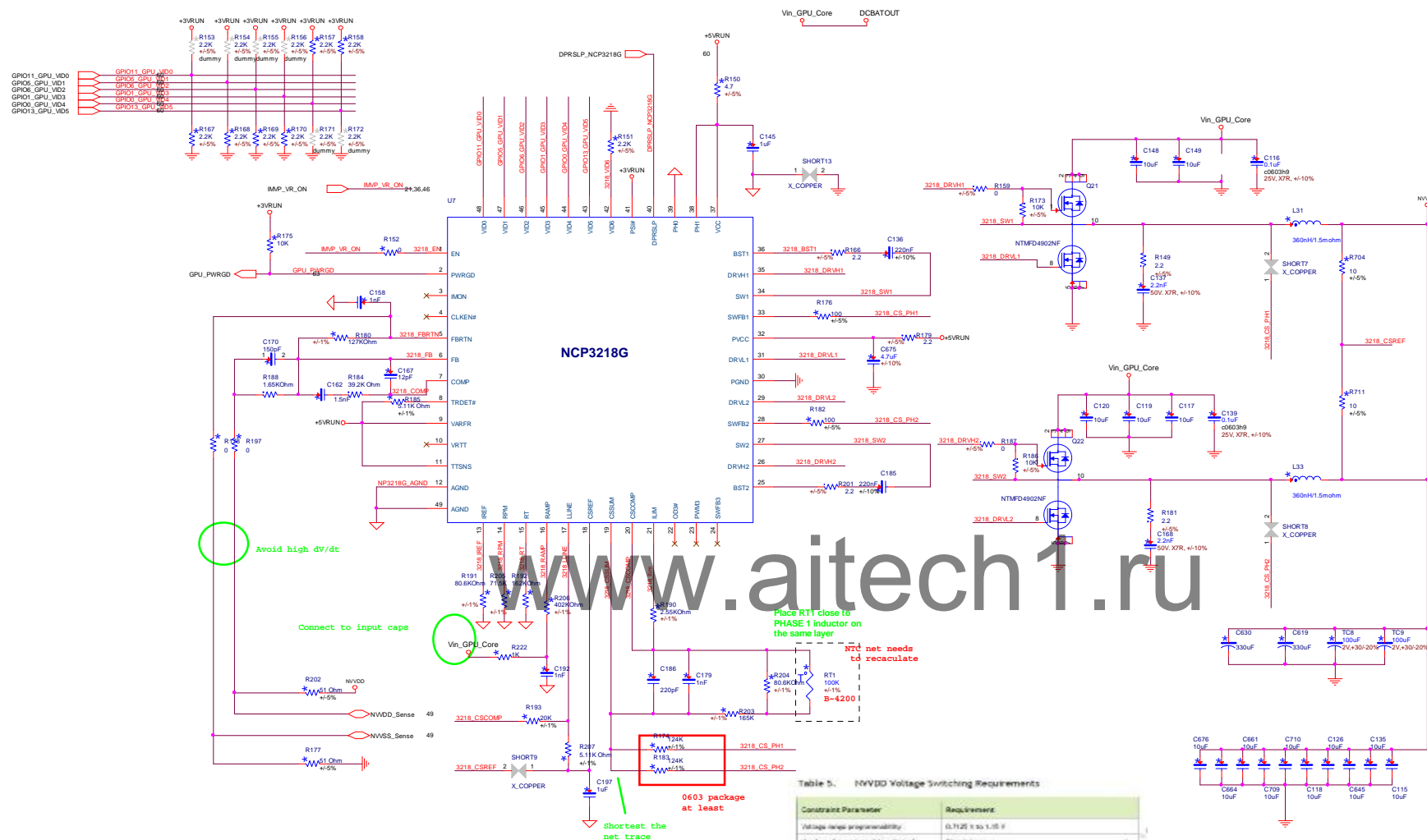
GPIO	Function	GPIO	Function
GPIO 0	Debug/Service Header/AIL_Fan PWM	EXPND 0	I2C PORT C
GPIO 1	VID 2	EXPND 1	Level Shifter Error Correction
GPIO 2	LCD brightness control (BL PWM)	EXPND 2	NVGEN GPIO EXP1/PS_Margin*
GPIO 3	LCD Power enable (PPEN)	EXPND 3	NVGEN GPIO EXP2/PS_MR*
GPIO 4	LCD Backlight enable (BLEN)	EXPND 4	GPIO_DEBUG_SERVICE HEADER
GPIO 5	VID 0		
GPIO 6	VID 1		
GPIO 7	3D STEREO		
GPIO 8	GPU Overtemp	EXPND 4	GPU_PS_EN
GPIO 9	GPU thermal Alert	EXPND 5	RSVD
GPIO 10	FB Vref Control (not used sDOR3)	EXPND 6	PEX_RST
GPIO 11	FBVDDQ VID (Reserved)	EXPND 7	RSVD
GPIO 12	PWR_Level AC Detect		
GPIO 13	PS1 Vpirm Enable		
GPIO 14	HPD for IFP AB (not used)		
GPIO 15	HPD for IFP C (HDMI DPA)		
GPIO 16	Run PWM control		
GPIO 17	HPD for IFP D (DP)		
GPIO 18	HPD for IFP E (DV/H DL)		
GPIO 19	HPD for IFP F (not used)		
GPIO 20	NVGEN Debug GPIO13		
GPIO 21	NVGEN Debug GPIO14		



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File			
GPIOs, Thermal Sensor, I2C/GPIO Expanders			
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NVVDD (PS1)PHASE 1&2 DRIVERS/FBVDD (PS2)



```
GPU 28W
IccTDC: 22A
Icc_continuous:24.42A
IccMax: 33A
VID: 0.7125V-1.15V
DC Ripple:±/2.5%
Transient:
    Vpp,150mV(20M), 200mV(1G)
    Icc_Dyn_VID1: 21.2A, 9.9A/uS
R_LL: ? mOhm
H/W Boot VID: 0.9V
OCP: 50A
```

Table 5. NVDD Voltage Switching Requirements

Constraint Parameter	Requirement
Voltage range programmability	0.125 to 5 to 1.05 V
Number of programmable voltages ²	56 voltages
Programmable voltage steps	12.5 mV
Voltage Regulation DC tolerance	± 2.5% or better
Voltage Regulation AC tolerance	Transient load: 150 mV/gk within 10 μs 0.5% High frequency ripple: 100 mV/gk with 100 kHz
Sim. Basis	2 mV/gk (± 0.1%) mV/gk
Setting "Time"	> 100 μs

- Notes:**
1. This logic is the voltage regulator results a minimum of 2.8mV_{DO}. To make the circuit simple, we recommend a 4.5V_{DO}.
 2. This applies to any logic switching, maximum I_{DD} controlling GPIO modules to reduce the power supply is installed in the desired voltage level. Figure 11 illustrates the I_{DD} vs. output logic view.
 3. This dependent on the volume within the 20ns the I_{DD} & GPIO I_{DD} dependence. Refer to PLS by any SOC specific more information.



Title		NVVDD (PS1)PHASE 1&2 DRIVERS/FBVDD (PS2)	
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Straps

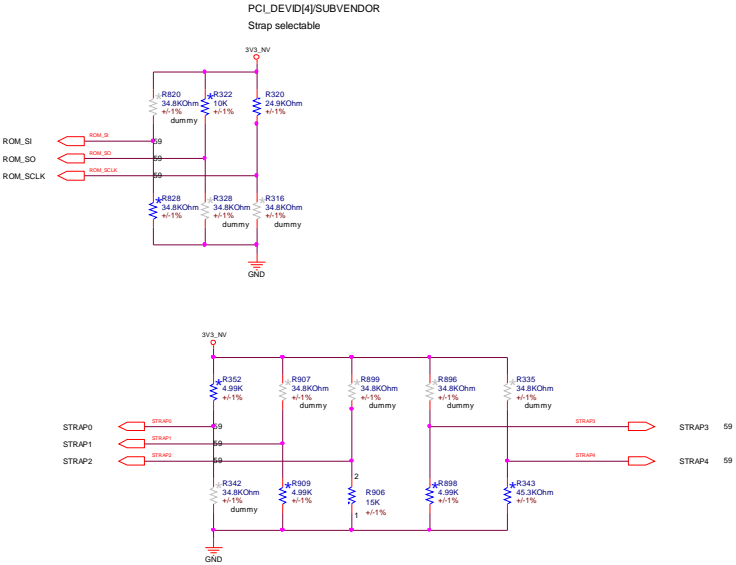


TABLE 1: STRAP DECODE ACCORDING TO
TERMINATION RESISTANCE/VOLTAGE

TERMINATION RESISTANCE	TERMINATION VOLTAGE	
	3V3 [3:0]	GND [3:0]
5K	1000 8	0000 0
10K	1001 9	0001 1
15K	1010 A	0010 2
20K	1011 B	0011 3
25K	1100 C	0100 4
30K	1101 D	0101 5
35K	1110 E	0110 6
45K	1111 F	0111 7

GF117/GK10X STRAP PIN MODE TABLE			
PIN NAME	MULTILEVEL bit [3:0]	BINARY PRODUCTION	BINARY BRINGUP
STRAP0	USER[3:0]		3GIO_PADCFG_LUT_ADR0
STRAP1	3GIO_PADCFG_ADR[3:0]		3GIO_PADCFG_LUT_ADR1
STRAP2	PCI_DEVID[3:0]		3GIO_PADCFG_LUT_ADR2
STRAP3	SOR[3:0]_EXPOSED		3GIO_PADCFG_LUT_ADR3
STRAP4	RSV, RSV, PCIE_MAX_SPEED, DP_PLL, VDD33V		PCIE_MAX_SPEED
ROM_SCLK	DEVID[4], SUB_VENDOR, DEVID[5], PEX_PLL_EN_TERM		SMB_ALT_ADDR
ROM_SI	RAMCFG[3:0]		SUB_VENDOR
ROM_SO	FB[1], BAR_SIZE, FB[0], BS, SMB_ALT_ADDR, VGA_DEVICE		VGA_DEVICE

NOTE 2: See table 1 for the correct value/location of the strap resistor for the desired modes
NOTE 3: Bring-up SKU(s) have jumper configurable subvendor and DEVID_4 settings see the ROM_SCLK STRAP


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FBVDDQ (PS3) FBVDD (PS2) DRIVER(Optional/Debug)

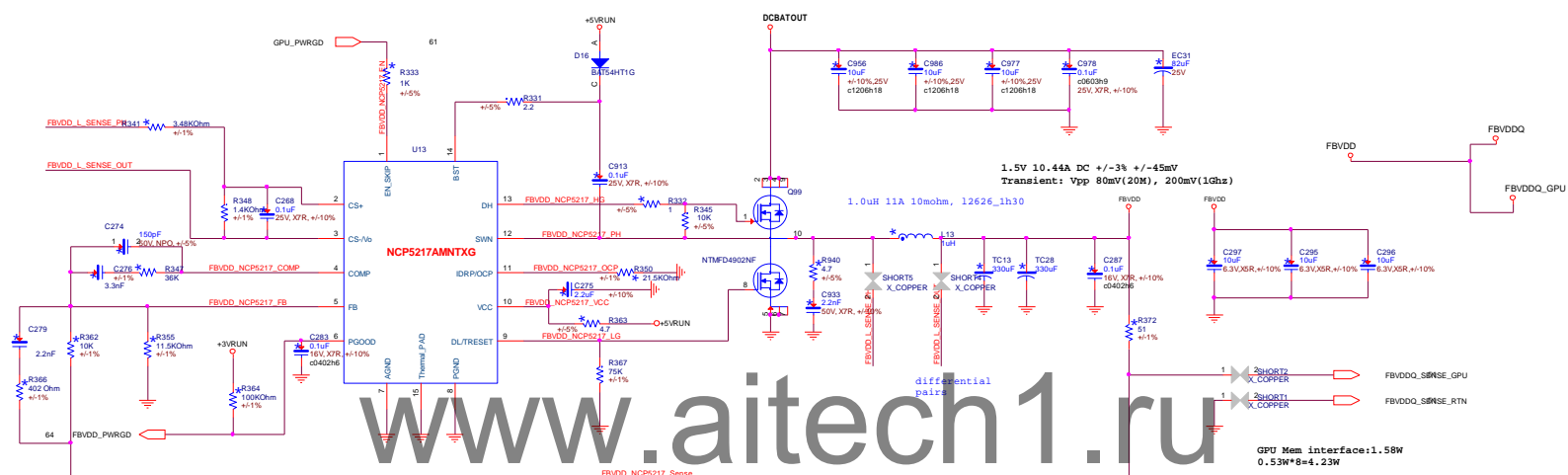


Table 23. Power Rail Requirements for DDR3 Frame Buffer Interface

Constraint Parameter	Requirement
FBVDDQ/FBVDD	1.5 V
DC tolerance	±3%
AC tolerance	Transient noise tolerance: 80 mV p-p within 20 MHz BW; high frequency noise tolerance: 200 mV p-p up to within 1 GHz BW
GPU FBVIEF ¹	internal VIEF
Memory FBVREF	0.5 x FBVDDQ

Notes: Since the GPU internal Vref is used, the TDD of pin on the GPU can be left unconnected.



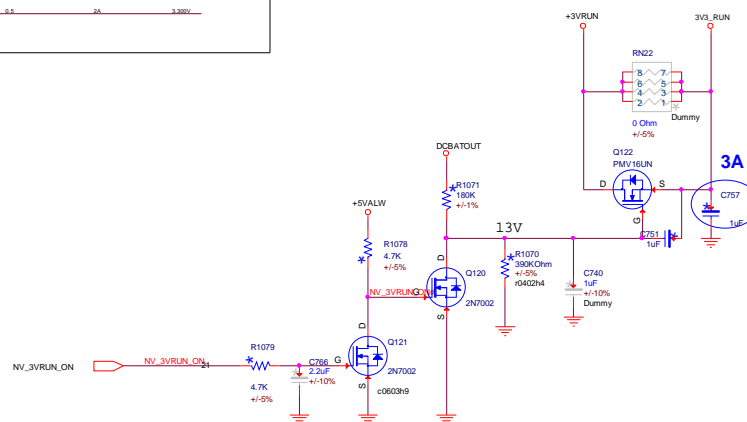
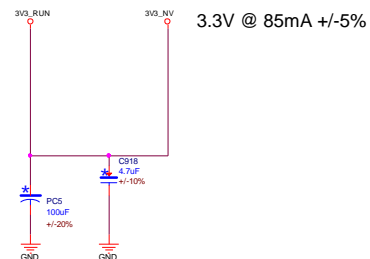
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Title		FBVDDQ (PS3) FBVDD (PS2) DRIVER(Optional/Debug)	
Size	Document Number	aNice	
Custom			

VBATT TO 3V3 SWITCHER

GLOBAL POWER CONSTRAINTS

NET	MIN_LINE_WIDTH	MAX_CURRENT	VOLTAGE
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PEX_VDD Switcher (PS5) and Miscellaneous Voltage Rails

changed to AOS MOSFET

PEX_VDD

3.0Amps @ 1.05V +/-30mV

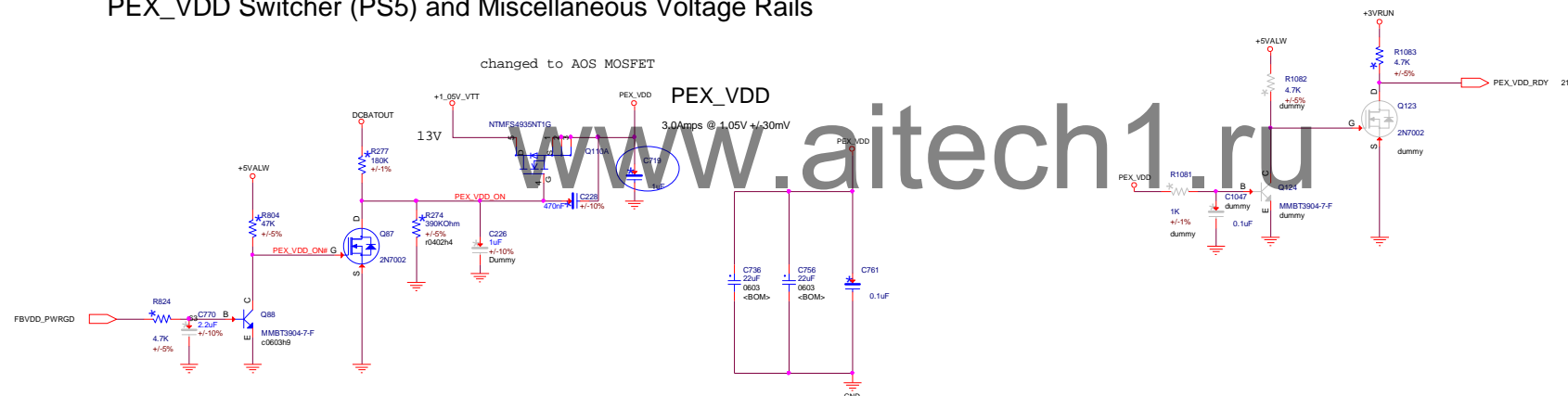


Table 27. GPU Frame Buffer PLL Power Rail Delivery

Power Rails	N13x Voltage Tolerance	Max Current Draw
FBx_PLL_AVDD + FB_DLL_AVDD	1.25 V \pm 30 mV	66 mA per partition on FBx_PLLAVDD, 35 mA on FB_DLL_AVDD

Note: The current values are estimated and are preliminary. Refer to the GPU-specific Electrical and Thermal Design Guidelines application note for further details.



FOXCONN PCEG

Title	5V/3.3V (PS4) Dual Switcher and 1V8 LDO (PS7)
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4

3

2

1

EC GPIO Map

Pin	Pin definition	Pin Net name	I/O Status	Memo
2	PSI_L/FAN_TC4/CIRRX2/GP15	PCHHOT_PCH#	NC	
3	SVD_O/PCIRSTIN#/CIRT2/GP15	SUSPWRDNACK		
6	GP63	AMP_PD#		
10	FAN_TAC2/GP52	SYS_PWROK_EC		
11	FAN_CTL2/GP51	Thermal_Alert		
12	FAN_CTL3/GP37	Audio_Source_Sel		
13	FAN_TAC3/GP36	EXTSMI#		
14	GP35	PM_SLP_S5#		
15	GP34	FW_HW#		
16	SVC_I/GP33	PM_SLP_S4#		
17	SVD_I/GP32	PM_SLP_S3#		
18	CORE_TYPE//GP31	SUS_PWRGD		
19	ATXPG/VID0/GP30	RUN_PWRGD		
20	SIN2/GP27	UART_TX		
21	SOUT2/GP26	UART_RX		
22	DSR2#/GP25	IMVP_OK		
23	RTS2#/GP24	Log_LED_CTL		
24	SI/GP23	SI		
25	SCK/GP22	SCK		
26	DCD2#/GP21	GPIO8_GPU_OVT*		
27	CTS2#/GP20	IMVP_VR_ON		
28	R12#/GP17	USB3.0_CTL3		
31	PCH_C1/SVC_0/GP14	PCH_C1		
32	PWROK1/GP13	ALW_ON		
33	PCIRTS1#/GP12	AC_PRESENT		
34	PCIRTS2#/GP11	ALW_PWRGD		
45	KRST#/GP62	H_RCIN#_D		
48	SO/GP50	SO		
56	GP76	OVI_EC#		
57	GP75	INT1_Proximity		
58	GP74	PM_SLP_W#		
59	GP73	INT_OSD		
60	GP72	WAKE_SCI#		
61	GP71	WLAN_EN		
62	GP70	PWR_ON_GPIO		
63	GP87	Disassociate_EC		
64	GP86	PCIE_WAKE#_EC		
65	IO_SCI#/GP85	RUNTIME_SCI#		
66	D_TX0/SMBDAT2/IRTX/GP47	SMBDAT2		
70	D_RX0/SMBCLK2/GP46/IRRX	SMBCLK2		
72	PWRON#/GP44	PWRON#		
73	PME#/GP54	USB3.0_EN		
75	PANSHW#/GP43	PANSHW#		
76	PSON#/GP42	PSON#		
77	SUSC#/GP53	EN_BLUT		
78	PWROK2/GP41	PM_PCH_PWROK		
79	3VSBSW#/GP40	RSTJ_From_EC_L		
80	KDAT/GP61	KDAT		
81	KCLK/GP60	KCLK		
82	MDAT/GP57	MDAT		
83	MCLK/GP56	MCLK		
84	PCIRST3#/GP10	RSMRST#		
85	RSMRST#/CIRRX1/GP55	CIRRX		
100	GP92/ADC2	NC		
101	GP93/ADC3	NC		
102	GP94/ADC4	NC		
103	GP95/ADC5	NC		

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